TDC-F1

High-performance 8-channel TDC

8 channels 120ps / 4 channels 60ps

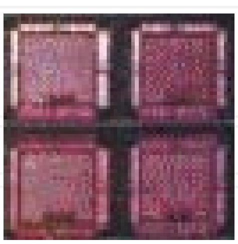
Functional description

scientific version

14.12.2001

acam - solutions in time

Precision Time Interval Measurement



Preface

Time is the most elementary physical dimension that we are familiar with. It is also the dimension which we can measure with the most precision. acam is specialized in designing integrated circuits and systems for high precision time interval measurement. The realization of these circuits became possible due to the progress in the semiconductor technology.

The F1 was developed on behalf of and in collaboration with the Faculty of Physics of the University of Freiburg, Germany, to fulfil tasks in experiments for high-energy physics, especially the COMPASS experiment. Some of the programming possibilities and measurement modes are very specific to the needs. Mainly the implemented trigger matching unit is dedicated to those experiments, where a low level of relevant data must be selected from intensive background signals at highest measurement rates.

If you're not sure whether your measurement task can be solved with the F1, please call our hotline (0721/966-4214 or support@acam.de). We guarantee that this phone line is hot and that your questions regarding the applications of the F1 are important to us. This is your chance to take advantage of these possibilities!

The newest information regarding our products can also be found on our web-page:

http://www.acam.de

This is still a preliminary edition. Are there any incorrect statements or points that should be explained more in detail? Do you have ideas for new topics to be implemented? If yes, please send us an email, we are open minded to every improvement.

acam-messelectronic gmbh, March 2000

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Index

Preface 2

Structure of the Manual 4

1 Short Introduction to TDC-F1 5

1.1 General Description 5
1.2 Key Features 5
1.3 Blockdiagram 6
1.4 Resolution Adjust 7
1.5 Measurement Modes 7

2 Details of the TDC-F1 9

2.1 Input Section 10
2.2 Measuring Unit and Resolution Adjust 11
2.3 Trigger Matching 13
Synch-Reset 13
2.4 Common Mode 17
2.5 Synchronous mode 19
2.6 Letra Mode 19
2.7 Hit Mode 20
2.8 High Resolution 21
2.9 Data Output 22
2.10 Serial Interface 24
2.11 DAC 25

3 Measuring Results 26

3.1 The Terms 'Precision' and 'Resolution' 26
3.2 Attainable Standard Deviations of the TDC-F1 26
3.3 Offset Errors of the TDC-F1 26
3.4 Systematic Errors of the TDC-F1 27
3.5 Histograms 27

4 Applications 30

5 Technical Data 30

5.1 Electrical characteristics 30
5.2 Absolute ratings 30
5.3 Current consumption 30
5.4 Timings 30
5.5 Package 33
5.6 Pinning 33
5.7 Pin description 34

6. Quick Reference 39

6.1 Electrical Characteristics 39
6.2 Pin Description 39
6.3 Timings 39
6.4 Registers 40

Structure of the Manual

The manual of the TDC-F1 is divided into 6 main sections. It is designed as an information and reference book for the advanced user.

The 6 main sections are:

- Short introduction to the TDC-F1

This section surveys the various functional possibilities the TDC-F1 offers without describing any details regarding the specific functions. You will find everything noteworthy in this section concerning principle applications and measurement problems. This section should be interesting for anyone who is dealing with the chip for the first time or who is interested in getting a brief overview regarding new developments and applications.

- Details of the TDC-F1

This section reveals in detail the various functions of the chip. The various application possibilities are described with precision. A developer can find information here regarding circuit and software design.

- Measuring results

All theory is gray. How good is the TDC-F1 in fact? This is where the F1 reveals it's skills as well as it's limits. This section of the manual is interesting for everyone, but especially for those customers who plan to - or have to - exhaust the chip's limits. It is also interesting for anyone looking to compare his own test results to ours. Are your measurement results clearly better or worse than ours, then call us or write us an email. We gladly give and receive tips.

- Applications

Will be filled with content in the future

- Technical Data

This section of the manual describes several specific examples regarding the circuit and controlling of the TDC-F1.

- Quick reference
- Latest main changes:

  April 2001: chapter 2.3 Trigger matching

  December 2001: chapter 2.5 Synchronous mode

1 Short Introduction to TDC-F1

1.1 General Description

The abbreviation TDC stands for Time to Digital Converter. These integrated circuits convert smallest time intervals into digital values at high resolution. Therefore they can be regarded in analogy to ADCs (Analogue to Digital Converter), which do the same with analog voltages. Although this definition would permit wrist watches or simple digital meters to be considered TDCs, the term 'TDC' is used only to describe high precision time measuring devices. Generally, a TDC describes a converter with a resolution less than one nanosecond. This high resolution cannot be achieved via meters or similar devices without high expenditures, so that new customized solutions become necessary.

The TDCs of acam are based on the use of digital delay times, employing purely digital-based processes (CMOS as a rule).

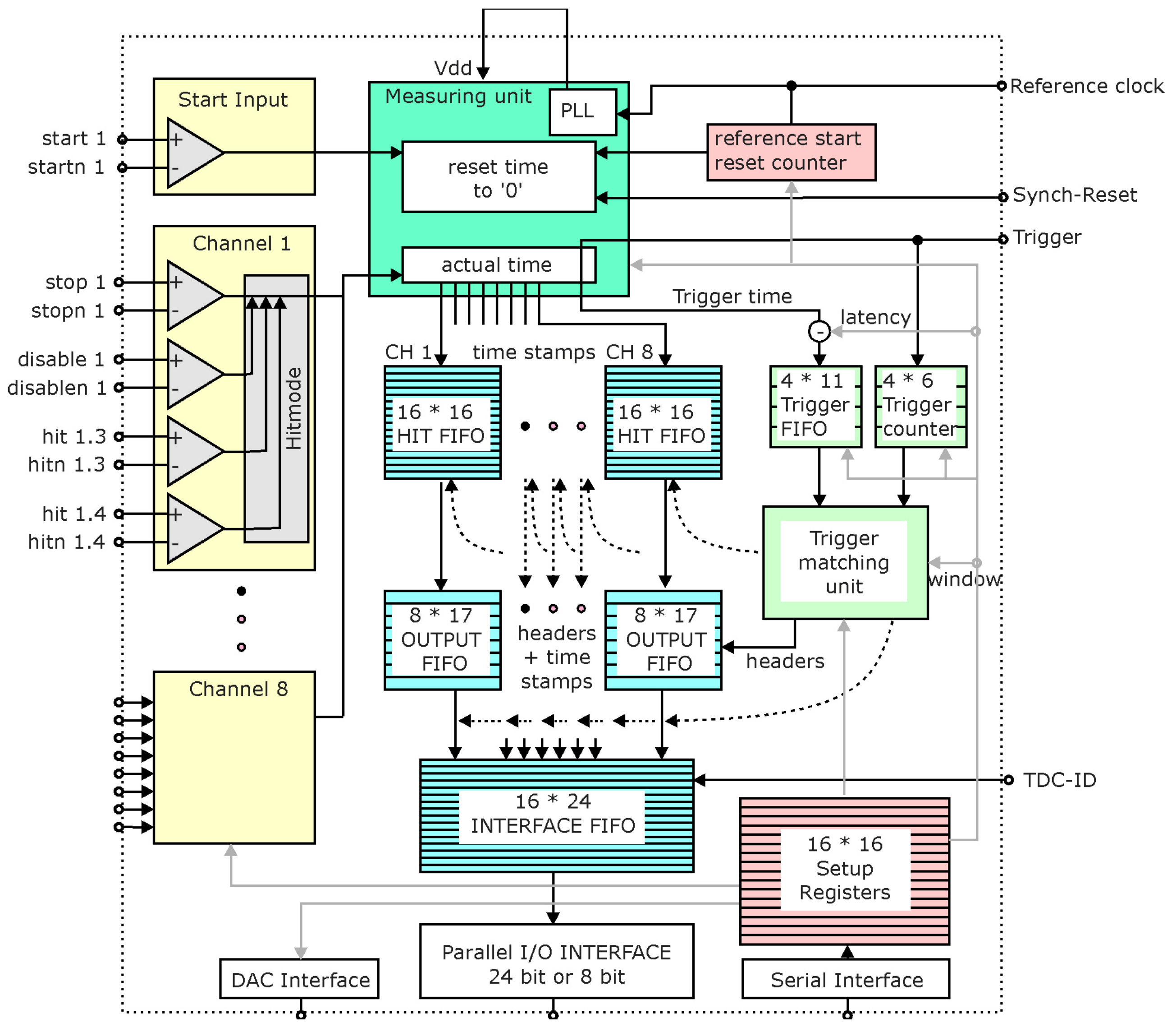
The TDC-F1, developed on behalf of and in collaboration with the University of Freiburg, offers 120 ps LSB width in normal resolution (8 channels) or 60 ps LSB width in high resolution mode (4 channels). The specialty of the TDC-F1 is a very complex trigger matching unit, that allows to suppress noise data and to filter out signals related to a trigger signal directly on chip. The result is a data-stream of only valid data and highest measurement rates up to 20MHz.

1.2 Key Features

- 8 channels with 120 ps resolution (LSB) each, resolution exactly the same for all channels, multihit capability, double pulse resolution typ. 20ns.
- or 4 measuring channels with 60 ps and multihit capability (High Resolution Mode)
- or 32-channel hit mode with typ. 4.6ns resolution
- Complex trigger-matching unit for on-chip data selection
- Measurement range 5ns - 7.8 µs (65535 LSBs) with normal resolution (Start-Stop measurement)
- Measurement range 5ns - 3.9 µs (65535 LSBs) in high resolution mode (Start-Stop measurement)
- Time differences between hits on different channels down to zero
- Resolution Adjust Mode: quartz-accurate, adjustable resolution ,insensitive to temperature variations, adjustable via software (no calibration necessary)
- Programmable edge sensitivities for all inputs: for time differences bigger than double pulse resolution the pulse width can be measured directly using one channel (sensitive to rising and falling edges)
- Disable input for each channel
- extremely fast data processing: depending on hit rate and data read-out unlimited multihit capability can be achieved.
- up to 7 results per channel can be stored
- Reference clock range between 1 MHz and 40 MHz
- compact 160 PQFP package (0.65 mm pitch)
- Industrial operating temperature range: -40 ºC ... +85 ºC
- Supply voltage: 2.7 V ... 5.5 V
- Low current consumption

1.3 Blockdiagram

Figure 1



1.4 Resolution Adjust

A very important feature of the TDC-F1 is the use of resolution adjust mode. In this mode the resolution of the TDC is quartz-accurately adjustable to a programmable value, simultaneously for all eight channels. As a reference for the regulation loop an internal clock is used which is derived from the external reference clock. The adjustment of the resolution happens via software by setting registers. The resulting resolution is defined by the programmer!

The resolution remains stable due to variations in the measurement core voltage, which is regulated by a PLL (Phase Locked Loop). The external circuit of the PLL regulation needs only a few small and cheap components. In this mode the resolution is not dependent on each single device anymore. It is independent from temperature and voltage and absolutely long-term stable (besides the temperature behaviour of the reference quartz). In this mode separate calibration is not necessary.

The adjustment range of the resolution can reach values from -30% up to +10% of the normal resolution at 5 V and 25°C. If environmental conditions lead to very large adjustments the locked-state can be lost. Then the PLL changes to floating resolution until the conditions allow the PLL to lock again. A status signal (pin 148) indicates whenever the F 1 is in a phase locked state.

1.5 Measurement Modes

The TDC-F1 is designed to fit the specifications for the COMPASS experiment at CERN. Different measuring modes had to be implemented to fulfill the requirements of various detectors in this experiment. For use in standard applications the common mode was added.

1.5.1 'Trigger Matching' Mode

It's the main feature of this mode, that from all the hits on the TDC only those are passed to the output FIFO that fit into a given trigger window. Hits arriving on the several inputs are stored in a first FIFO, the 'HIT FIFO'. Up to 16 hits can be stored in this FIFO. As soon as a trigger signal is sent to the TDC, the values in the HIT FIFO are checked for their validity. The validity is defined by trigger latency and trigger window width. The trigger matching unit goes back in time (latency) and looks for all values fitting to the trigger window. These are then transferred to the next FIFO, the 'OUTPUT FIFO', which can store up to 8 values. All hits older than trigger latency will be deleted from the HIT FIFO. The other data will be kept and may be used for the next trigger matching. The triggers are counted internally and the trigger number is added to the hit values. Trigger matching starts with channel 1 and ends with channel 8. When trigger matching for all channels is completed, the data are transferred from the OUTPUT FIFO to the INTERFACE FIFO. The trigger matching is 'switched of' setting the common mode.

1.5.2 'Common' or 'Start / Stop' Mode

In common mode standard start-stop measurements can be done. All data are transferred to the output 'unfiltered'. The maximum time interval between start and stop hit may be 7.8µs in normal, 3.9µs in high resolution mode.

As in trigger matching mode, the measuring unit is running all the time. The time reference is set to '0' with every hit on the start input. The TDC-F1 will accept hits at any time, even without a start hit, but these values don't make any sense, as they refer to an arbitrary reference time. If stop hits arriving later than the maximum of the measurement range, the measuring unit will start from zero and the time stamps will be wrong. If the experimental setup allows hits outside the measurement range, the stop inputs must be disabled.

For reason of the TDC-design, also in common mode an internal trigger matching is performed every typ. 150ns. But in common mode all data present in the HIT FIFO are transferred to the OUTPUT FIFO. This internal trigger matching will reduce the maximum measurement rate to 1-2MHz.

1.5.3 'Synchronous' Mode

In the original experimental setup, the TDC-F1 is designed for, trigger matching is combined with the synchronous mode. The Synchronous mode is operating similarly to a predivider for extension of the measurement range of the TDC-F1. It can be used for measurement tasks with time intervals longer than

7.8µs in combination with an external circuit. In this mode there is no external start signal. A SYNCRES pulse (pin 52) generates an internal start that is synchronous to the reference clock. Afterwards the TDC-F1 is generating it's own start signals in constant time intervals. The interval between starts can be programmed in multiples of the reference clock (register7 Refcnt).

This mode cannot be used without external logic circuitry.

1.5.4 'Leading-Trailing' mode

Another mode specific to high energy physics is the leading-trailing mode. In this mode every channel is sensitive to rising and falling edges. Additionally to the time measurement the kind of slope (rising or falling) is stored. The lowest one of the 16 data bits indicates the slope. The resolution is bisected.

1.5.5 'Hit' or 'Latch' Mode

The hit mode is intended for roughly time measurements on a lot of measurement channels. The number of channels is increased to 32. In this mode the stop inputs, the disable inputs and the two additional hit inputs of each channel are combined with an or-function into one channel. The arrival of the first hit on any of these four inputs starts an internal programmable timer, that initializes an internal hit on this channel. The lowest four bit of the measurement result are overwritten by the hit registration of the four inputs.

1.5.6 High Resolution

The complex chip design allows to combine channels in pairs. This way the resolution is improved by a factor of 2. The number of usable channels is reduced to 4, the resolution per channel is typ. 60ps. The even numbered channels are internally disabled (but they must be enabled by hardware, disable pins to GND). The principal timings remain the same, except the measurement range which is reduced to 3.9µs. Both HIT FIFOs of the combined channels will be used. As a result the data capability per channel is doubled. High measurement rates are possible. The results are written to HIT FIFOs n and n+1 (means 1+2, 3+4, 5+6, 7+8) in an alternating manner. In the output data of neighbored channels belong together.

1.6 Data Transfer

The TDC-F1 is set up via a serial interface. All necessary adjustments are done by setting 16 configuration registers of 16 bit each.

The link to a receiver of TDC data is either realized via an 8 Bit HOTLink protocol with a maximum transmission rate of up to 50 MHz or directly via a 24 bit bus architecture, which can be clocked with a frequency of up to 50MHz. For the data transfer by HOTLink the 24 bit hit information is split in three 8 bit words.

For each hit a 24 bit data word is sent, including the 16 bit time stamp, the chip address and the channel address. In hit mode the least four bits of the time stamp define the wire address. In addition to the data word a 24 bit header word (or trailer word) can be sent, containing the event number and the trigger time. The output of a header and/or trailer word can be defined for each channel separately. Header words don't make any sense in common mode.

1.7 DAC

An add-on is the serial interface for programming an external, octal digital-to-analog converter (AD8842). This may be used to set the individual trigger levels of the 8 differential inputs.

2 Details of the TDC-F1

In this chapter we will describe every relevant function in detail. The appropriate adjustments will be discussed. Relevant registers are shown in their complete contents, when the function is explained. As far as possible the combination of several functions is described. This chapter is a must for everybody, who designs hardware implementing the TDC-F1 or who writes his own software.

Before operating the TDC-F1 must be prepared by setting the register contents in a correct manner according to the chosen measurement mode. The complete register structure is shown in Table 1: Register overview. The meanings of the various variables will be explained in the relevant sections.

Table 1: Register overview

Addr	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	headen								trailen							
1	hires	hitm	letra	sq		fake	ovlap	ibs		obsp	m_in	slow				DA
2	fe2	re2	adjch2						fe1	re1	adjch1					
3	fe4	re4	adjch4						fe3	re3	adjch3					
4	fe6	re6	adjch6						fe5	re5	adjch5					
5	fe8	re8	adjch8						fe7	re7	adjch7					
6	busclkdel				adjch10						adjch9					
7	beini	refcnt									hitt					
8	trigwin															
9	triglat															
10	don1	pll	track	neg	r_adj	refclkdiv			hsdiv							
11	dac 2								dac 1							
12	dac 4								dac 3							
13	dac 6								dac 5							
14	dac 8								dac 7							
15	don2	htest	stest	-	-	-	-	-	dia3	dia2	dia1	dia0	rosta	sync	com	8/24

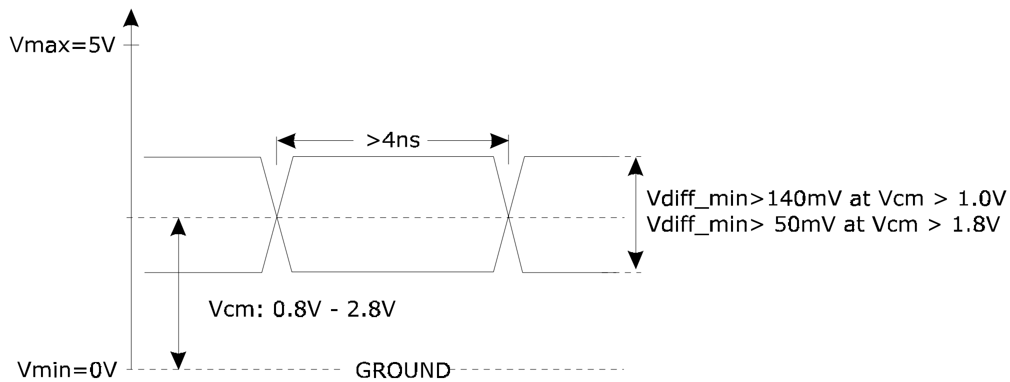
The configuration must be done in the right order, step by step:

1. After Power-Up-Reset (low active pulse >100ns at pin 47) first start the measurement core by setting **register 15** (rosta=1).
2. It is recommended to set in a next step the adjustments for resolution adjust mode in **register 10**: The values the reference clock divider (refclkdiv) and the divider for the measurement core (Highspeed-Divider hsdiv) have to be set depending on the external reference clock and the required resolution. Moreover the polarity of the output signal for the external voltage regulator (N-ph) is set. The whole thing is activated by setting bit r_adj to '1'. (see
3. 2.2 Measuring Unit and Resolution Adjust)
4. Set all other registers.
5. Finally set the init flag (Beini), **register 7,** to '1' to initialize all units.

2.1 Input Section

The TDC-F1 has 8 independent stop inputs and a common start input. These universal Low-voltage Pseudo-ECL inputs (LVPECL) can accept single ended or differential input signals. For single ended operation a variable threshold voltage can be applied to the inverting input. Figure 2 shows the necessary input levels.

Figure 2 : Input levels



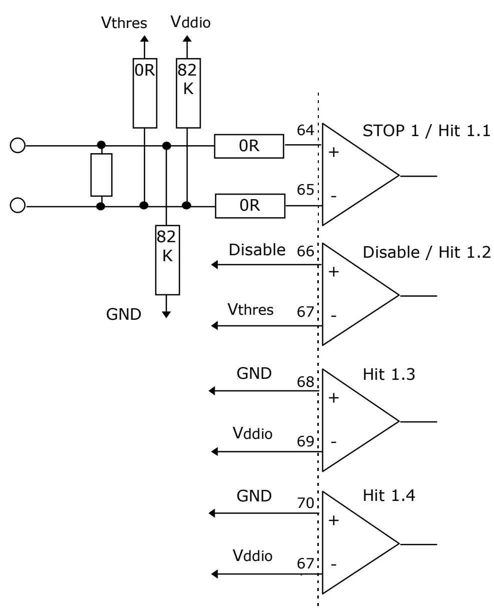
Inputs that are not used should be disabled connecting the non-inverting input to GND and the inverting input to Vddio.

The minimum pulse width is typ. 2.5ns (max. 4ns). The double pulse resolution on each channel is typ. 20ns (max. 30ns). Any signal arriving during the recovery time of the input interface will be ignored.

To each stop input there is also a differential disable input available. To enable an input permanently, the positive disable input should be connected to GND, the negative input to Vddio. The disable input is designed to be used at the setup. If it is used during measuring, it must be guaranteed, that no stop hits arrive in a time window 3 - 8 ns before the disable signal. If the time interval is less than 3ns the hit will be discarded, if the time interval is more than 8 ns the hit will pass. Otherwise disturbed measurements may occur. In this case an external disable is necessary.

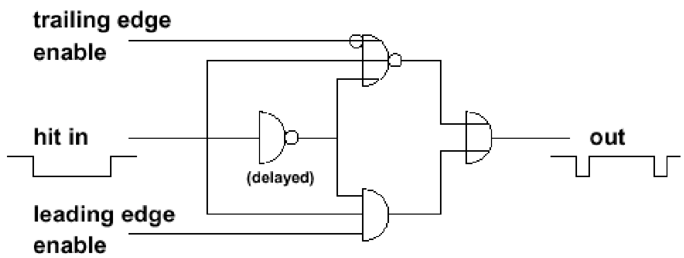
Alternatively all hits can be disabled via software (register 1, bit 5).

Figure 3: typical external connection



A programmable edge detection circuit (Figure 4) is realized to perform measurements either on leading edge, trailing edge or on both edges of a signal. It is possible to measure directly the pulse width, taking into consideration the double pulse resolution. If pulses are expected to be shorter than 30 ns, two neighbored channels can be combined and programmed in such way that one is sensitive to the leading edge and the other to the trailing edge. Now the only limitation is the minimum pulse width (4ns) of the input buffers.

Figure 4 : Slope control



Relevant registers:	
Registers:	2,3,4,5
Bit 6,14:	re x = enable sensitivity to rising ('leading') edge
Bit 7,15:	fe x = enable sensitivity to falling ('trailing') edge
Register:	1
Bit 5:	Disable of stop inputs

2.2 Measuring Unit and Resolution Adjust

The heart of the TDC is an asymmetric ring oszillator representing the actual time in a 17 bit value. The 17^{th} bit is only for internal use.

Depending on the measurement mode there are several possibilities to reset the ring-oszillator to '0':

- giving a signal to the start input (common mode)
- by use of the internal reference time reset counter (trigger mode). This programmable counter resets the measuring core after n cycles of the reference clock (n: refstart counter, register 7, bits 6-14)
- giving an synchronous reset (pin 52)

The measuring unit has a dynamic range of 16 bits, which is typically 65536 * 120 ps = 7.86µs. If the measuring unit isn't reset within this time, it will roll over and start from '0' again. The rollover is not indicated by the TDC-F1.

All time stamps, for hits on the stop inputs or the trigger input, are related to the 'internal start', the time when the measuring unit was reset. The time stamps for hits on the stop inputs are transferred to the 16 * 16 bit Hit FIFO for further processing. If the Hit FIFO is full, no further hits are accepted. The overflow is indicated at pin 145.

In principle the high resolution of the F1 is derived from the internal 'gate propagation times'. The gate propagation time is dependent upon voltage, temperature and the manufacturing process. Due to this dependency the resolution normally is not known and must first be calculated via calibration measurements. In addition, the resolution is not stable, it sways with voltage and temperature. This does not apply using the resolution adjust mode for the F1. In this mode the resolution of the F1 is adjusted quartz-accurately and absolutely temperature stable via Phase Locked Loop (Figure 5). The phase locked loop (PLL) regulates the core voltage of the F1 so that the resolution is set exactly to the value programmed.

The resolution is calculated as follows: $resolution = \frac{T_{ref} * 2^{refclkdiv}}{152 * hsdiv}$ refclkdiv, hsdiv → register 10

Example:

Reference clock = 40MHz → T_{ref} = 25ns

Divider for reference clock refclkdiv = 7 → 2^7 = 128

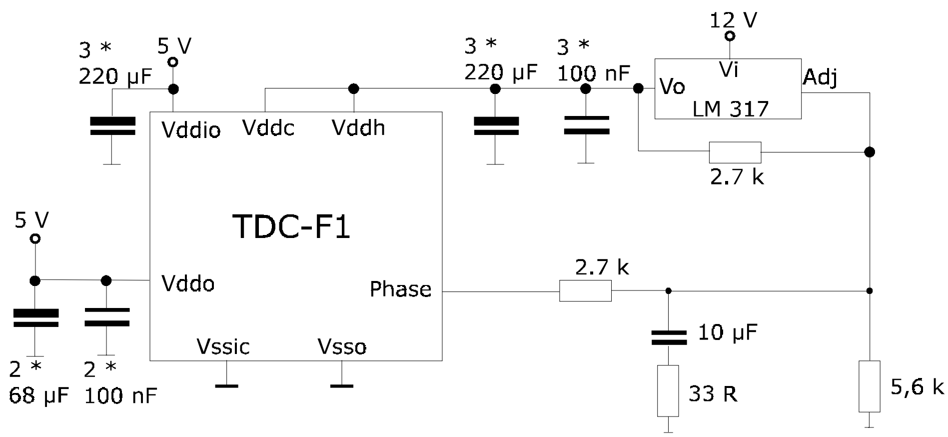
Highspeed divider hsdiv = 190

Using these values the resolution is set to 110.8ps in normal resolution or 55.4ps in high resolution.

The adjustment range of the resolution can reach values from -30% up to +10% of the normal resolution at 5 V and 25°C. If environmental conditions lead to very large adjustments the locked-state can be lost. Then the PLL changes to floating resolution until the conditions allow the PLL to lock again.

Figure 5 shows the recommended external circuit for the regulation loop. A very low cost regulator like the LM317 will work perfectly.

Figure 5 : External circuit for resolution adjust



Supply voltage

Although the TDC-F1 is a fully digital circuit, some analogue measures affect the circuit. The reason is that the TDC is based on the internal analogue measure 'propagation delay time' which is influenced by temperature and supply voltage. A good layout of the supply voltage is essential for good measurement results. It should be high capacitive and of low inductance. Use three capacitors of 150µF and three 100nF capacitors for the supply of the core (Vddc and Vddh). The pad ring supply should be stabilized by three 100nF capacitors. The supply of the strong outputs (Vddo for pins 1 - 40) should be blocked with two 68µF capacitors and two 100nF capacitors (When opening the output buffers the current consumption may be very high).

There are several connections for power supply provided at the TDC-F1:

- Vsso - Ground for the strong outputs
- Vddo - Supply for the strong outputs
- Vddc - Supply for the core (floating by the resolution adjust regulator)
- Vddh - Supply for measurement unit (externally connected to VDDC)
- Vddio - Supply for pad ring
- Vssic - Ground for pad ring and core

The supply voltage for the core should not be higher than the supply voltage of the pad ring plus 0.5V. Otherwise the signal flow could be disturbed. A core voltage Vddc that is 300-500mV higher than the measuring unit's voltage Vddh will improve the standard deviation of measurements.

All ground pins should be connected in a central point on the printed circuit board. Vddc and Vddh are floating and are supplied from the resolution adjust voltage regulator. Vddio should be provided by a fixed voltage regulator to avoid disturbances caused by the inputs supply. There is no special instruction for Vddo. It can be connected externally to Vddio.

Relevant registers:

Register:	10
Bit 0-7:	hsdiv = high speed divider, 0-255
Bit 8-10:	refclkdiv = reference clock divider (possible factors: 1, 2, 4 ... 128)
Bit 11:	r_adj, '1' = switch on resolution adjust mode
Bit 12:	negphase, inverts phase output of PLL, must be set to '1' for the circuit Figure 5
Bit 13:	track, '1' breaks PLL loop (for test only)
Bit 14:	pll, diagnosis of PLL. Pin 148, lock, indicates, going to 'High', that the PLL is locked.
Register:	1
Bits1-4,6,7-8:	Transfer-speed between buffers, default = '0' = fastest (leave as is!)
Bit 11,12:	Correction of strong production lot variations, default = '0' don't touch!!
Register:	15
Bit 3:	rosta, '1' = start ring oszillator (must be set to '1')

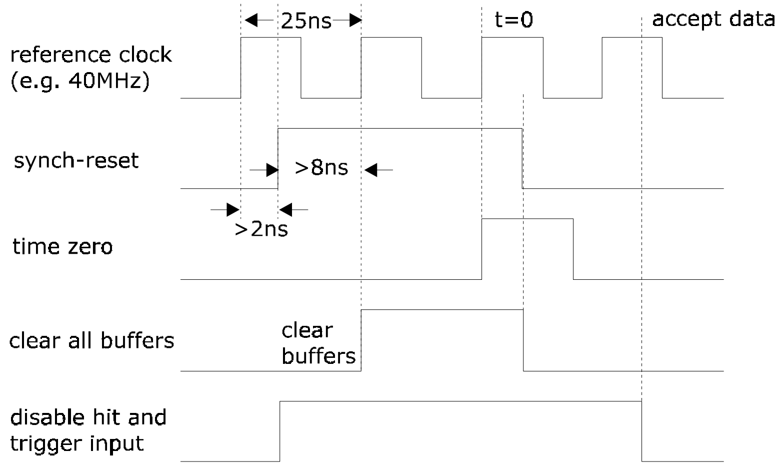
2.3 Trigger Matching

In the following we will always refer to trigger matching in combination with synchronous mode. In this mode all time measurements are measurements relative to the last synchronous reset of the module modulo Tref*refcnt. All measured times are stored in a hit FIFO. An external trigger signal starts the trigger matching unit, which selects relevant data from the hit FIFO and transfers them to the output FIFO. Relevant data are defined by two parameters: trigger latency and trigger window width. All data corresponding to a trigger are identified by an event (or trigger) number in the header word. If the time of a trigger signal is known (from an external circuit), the times for all the hits can be calculated in respect to the synchronous reset.

Synch-Reset

In a typical experiment a well defined simultaneous reset for all TDCs is necessary for successful event reconstruction. This can only be guaranteed if the synch-reset signal arrives at the TDC synch-reset pin (pin 52) at least 2 ns after a positive edge of a reference clock cycle and at least 8 ns before the next positive edge of a reference clock cycle is reached. Figure 6 shows these timing requirements for a 40 MHz reference clock. Hits arriving within the first clock cycle after a synch-reset signal will have a wrong time stamp and should be ignored in data analysis. Thereafter no such limitations have to be regarded.

Figure 6 : Synchronous reset



The synchronous reset sets the measuring unit to time=0. It is reset to zero repeatedly after the configured number of cycles of the reference clock is reached. So the full time scale is divided into so called 'frames'. The number of cycles is set in register 7, bits 6-14 ('refcnt'). The start input must be disabled, connecting start (pin 61) to ground and startn (pin 62) to Vddio.

*Example: given a reference clock of 40MHz and refcnt set to 100, all timings refer to the synch_reset pulse modular in 20*25ns = 500ns.*

Hit no.	*time after synch_reset*	*time stamp in hit buffer*
1	*50ns*	*50ns*
2	*450ns*	*450ns*
3	*700ns*	*200ns*

Trigger Matching

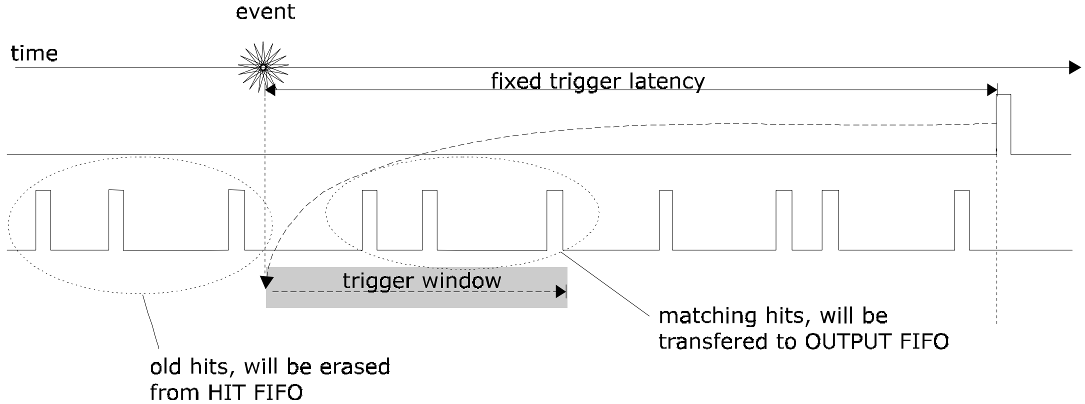
The key feature of the TDC-F1 is it's complex trigger matching unit. In the COMPASS experiment, for which the F1 was designed, only a small portion of the events and the corresponding hits on the TDC are of interest. Due to the large number of detectors and therefore a very high data rate, it is necessary to preprocess the data and select only relevant data for transfer. A separate electronic unit (Trigger Control System TCS) decides, whether an event is relevant or not. This valuation needs it's time. So when the TCS sends a trigger signal, this trigger is related to data in the past. The time between a relevant event and the trigger signal is called trigger latency and is fix for an experimental setup. In addition the trigger window defines the time slot after this event, in which relevant hits may occur.

Trigger latency = register 8 * resolution + 25ns
Trigger window = register 9 * resolution

When the TDC-F1 receives a trigger, two things happen in a first step:

- the trigger time is roughly measured with typ. 4.6ns resolution, 11 bits wide, and transferred to a 4-register trigger FIFO. The trigger FIFO in combination with the output FIFO and interface FIFO allows to handle multiple triggers at once. The number of intermediately stored triggers is dependent on the hit rate and ranges from min. 5 (events with many hits) to max. 13 (hitless events). If the trigger FIFO is full, no further triggers will be accepted, but the trigger counter will continue. So even if a trigger is lost, the next accepted one will have the right trigger number. A trigger overflow is indicated in bit 22 of the header/trailer. The corresponding header is forced to be read out.
- a 6-bit trigger counter is incremented and the value is transferred to a 4-register counter FIFO. The trigger (or 'event') counter allows a clear identification of the data.

Figure 7 : Trigger matching



As soon as a trigger is in the trigger FIFO, the trigger matching unit starts it's work. The trigger matching is done for all channels simultaneously. Normally, first a header word will be written to output FIFO, containing event number, trigger time, chip address and channel. This header functions as an event separator in the data stream. Then the hit FIFO is queried for time stamps fitting into the related trigger window. The search mechanism uses two independent pointers. The read-pointer specifies the memory address currently being accessed. The start-search-pointer marks the address where the search is supposed to start when the next trigger is loaded from the trigger FIFO. When the first hit matching a trigger window is found, the start-search-pointer is set to the current read-pointer position. All hits previous to this particular hit are deleted because they are too old and out of the future regions of interest. The selected hit is copied to the output buffer. The read pointer is moved to the next addresses to look for further hits and, if successful, to transfer them to the hit output FIFO. The search stops at time stamps younger than the trigger window limit. In each channels hit FIFO the time stamps are stored in a strongly chronological manner (see Figure 8).

It is guaranteed that the trigger matching will work also if the trigger window overlaps two frames.

For a clear association of time stamps with triggers (events) and due to the lower resolution in trigger time the following timings must be taken into consideration:

trigger latency < 90% * Tframe (Tframe = Tref * refcnt)

trigger window width < 40% * Tframe

Because the output FIFO has 8 memory cells and one is occupied by the header word, the maximum number of hits related to an event is 7. In other words : maximum 7 hits can be extracted from the 16 hits in the HIT FIFO. In case the output FIFO is full and the trigger matching process is not completed, the remaining hits will be lost. When new space in the OUTPUT FIFO becomes available, an error word (Hex FFFF) is created and stored in the OUTPUT FIFO in the same format as normal data, appended to the last event. In addition the OUTPUT FIFO overflow pin (pin 151) is set to flag this state by hardware.

Figure 8 : Occupancy HIT FIFO

1	t2		400ns	
2	t1		200ns	
3	t0	oldest time	100ns	
4	t15	most recent time	3000ns	← write pointer
5	t14		2550ns	
6	t13		2500ns	
7	t12		1800ns	
8	t11	first time not matching to trigger window	1520ns	← read pointer
9	t10		1450ns	
10	t9		1400ns	
11	t8		1310ns	
12	t7	oldest time matching to trigger window	1200ns	← start search pointer
13	t6		1000ns	
14	t5		890ns	
15	t4		650ns	
16	t3	fourth oldest time	500ns	

The time needed for trigger matching is (time between trigger and valid (typ.)):

$$TtoValid = 200ns + nmax*35ns + (n+10+nt)*43ns$$

nmax = largest number of hits on any of the channels (Hit FIFO)

n = number of hits reffering to the actual trigger

nt = number of channels with trailor enabled

If for a longer period of time no triggers have arrived, the write-pointer may catch up with the start-search-pointer and the hit FIFO runs full. If then a new hit is received, the hit FIFO would not accept this hit and this time measurement would be lost. Regular fake triggers are generated internally to prevent this. Synchronously to the external reference clock a 6 Bit counter is continuously incremented. Whenever this counter overruns and the trigger matching unit is idle and no trigger is in the trigger FIFO, then a fake trigger is generated. The fake trigger is handled like any real trigger except that for a fake trigger no data are copied to the output FIFO. The generation of fake triggers helps to clean-up the hit FIFO from old hits and guarantees unambiguous time measurements. At initialization the time span for the generation of fake triggers can be selected to half the nominal value (register 1, bit 10).

In a final step all data for this particular event are transferred from the output FIFOs to the interface FIFO (16 * 24bits) channel by channel, starting with channel 1. The data-valid pin (pin 2) flags the readiness of the TDC to accept a readout token as soon as the interface FIFO is full or all data of an event have been transmitted from the eight OUTPUT FIFOs to the interface FIFO. The readout history register, the OUTPUT FIFO and the interface FIFO are always cleared at Power-up and during a synch-reset.

Meanwhile the next trigger from the TRIGGER FIFO is loaded from the trigger matching unit and will be processed.

Header / Trailer

When data are transmitted from the OUTPUT FIFO to the interface FIFO specific channel information is added. To each header and each data word seven additional bits are added: three bits for channel address and three bits for TDC address. Each TDC-F1 can have a 3-bit ID (0...7), coded by 'chipad' pins 44-46,

For event headers and trailers the seventh bit is generated from an exclusive Or of the setup registers. It is used to cross-check for Single-Event-Upsets in these important registers.

Header / Trailer word	0	1 Bit Trigger FIFO overflow	6 Bit Event number	9 Bit Trigger time	1 Bit Xor setup register	3 Bit Chip address	3 Bit Channel address

data word time measurement	1	0	3 Bit Chip address	3 Bit Channel address	16 Bit Time

Xor setup register: This bit is implemented to detect, whether one of the setup register bits has changed, e.g. due to strong radiation. As soon as one bit is changing, also this bit is changing.

For each channel one can define whether a header and/or a trailer word will be added to the data related to a particular event. They are necessary as event separators in the data stream. But they also cover memory space in the OUTPUT FIFOs. A good compromise is to enable a header on channel 1 and a trailer on channel 8. For the other channels header and trailer are disabled. As it is guaranteed, that the data output starts with channel 1 and ends with channel 8, The header and trailer enclose all the data to this particular event.

header
first hit channel 1
..
..
..
last hit channel 8
trailer

Relevant registers:

Register:	0
Bits 0-7:	trailer enable for each channel
Bits 8-15:	header enable for each channel
Register:	1
Bit 10:	halve the time interval for fake triggers
Register:	8
Bits 0-15:	width of trigger window
Register:	9
Bits 0-15:	trigger latency

2.4 Common Mode

The simplest operation mode of the TDC-F1 is the common mode, performing straight start-stop-measurements without trigger matching. All time stamps are transferred to the Interface FIFO. In this mode the TDC works best in combination with an external FIFO.

The configuration for this must be done in the right order, step by step:

1.) After Power-Up-Reset (low active pulse >100ns at pin 47) first start the measurement core by setting register 15 (rosta=1), adjust common mode (common=1), and select a bus width (BUS824=1 means 8 bit width; BUS824=0 means 24 bit width).

2.) Adjustments for resolution adjust mode in register 10: The values the reference clock divider (Ref-Clk Div.) and the divider for the measurement core (Highspeed-Divider) have to be set depending on the external reference clock and the required resolution. Moreover the polarity of the output signal for the external voltage regulator (N-ph) is set. The whole thing is activated by setting bit r_adj to '1'.

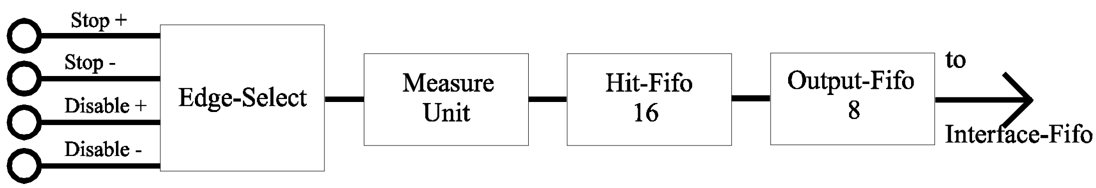
3.) In register 1 you choose between normal and high resolution. highres=1 means high resolution, highres=0 means standard resolution. Set all the other bits in this register to '0'.

4.) Registers 2 - 5 are responsible for the edge sensitivity of the inputs and the adjust values for the channels, necessary when high resolution mode is used. The fen bits choose falling edge, the ren bits select rising edge. Setting the mentioned bits to '1' enables the corresponding slope sensitivity. If none of the bits for one channel is set, this channel is disabled. The adjust bits (Adjust) for high resolution mode have to set to 111111 bin = 3F hex for channels 1, 3, 5, 7 and 9 (see 2.8 High Resolution).

5.) Finally set the init flag (Beinit), register 7, to '1' to initialise all units.

Implementing this configuration the TDC-F1 will run in common mode. Every incoming stop will be set in relation to the last start. The result in combination with the channel number will be given out immediately.

Structure of a measurement channel:



Parameters of a channel:

- Double pulse resolution (typ): 20ns
- Normal resolution (typ.): 120ps
- High resolution (typ): 60ps
- Dead time between start and stop (typ): 5ns

Hit FIFOs and Triggering

For a first memory storage all channels of TDC-F1 have their own 16-fold hit FIFOs. All data from the Hit FIFO will be transferred to the output FIFO. As the TDC-F1 initially was designed to perform trigger matching, the procedure to shift data from hit to output FIFO is an internal trigger matching, that doesn't filter any data. The TCD-F1 is checking continuously whether a hit is present. As soon as the first hit has arrived, the TDC-F1 writes a header into the output FIFO of each channel. 8 memory cells are available to each channel for the headers and the data. After registration of the header all incoming data is written to the belonging channel output FIFO. If the time interval between two incoming hits is larger than about 150ns, a new trigger matching is started, creating a new header. When using common mode there is no information in these headers, they should be suppressed. Setting register 0 to '0' suppresses the forwarding of headers and trailers (default = 0) from the output FIFO to the Interface FIFO.

The trigger matching is controlled internally. No parameters must be set. The internal trigger matching doesn't suppress any data. But as the trigger matching needs it's time, the measurement rate in common mode will be decreased to about 2 million measurements per second maximum.

In this mode trigger-in, pin 48 should be connected to GND. Connection to Vdd will disable the internal trigger matching.

Output FIFOs and Interface FIFO

The data is stored in channel's 8-fold output FIFOs in strictly chronological order. Depending on the measurement rate it is separated by headers. If the output FIFO is full and another hit is coming from the hit FIFO, this hit will be neglected and the output overflow flag is set. This flag is available at pin 151.

Due to the internal use of the trigger matching unit, the multihit capability is strongly dependent on the measuring rate. In best case, for low measurement rate e.g., the multihit capability is unlimited. In worst case, there is a header to each hit. Only four hits together with their header can be stored in the output FIFO. Further hits will be lost until the F1 is read out.

The TDC-F1 is giving out blocks of data. A block consists of the data of all channels between two headers. The data of all channels are joined together in the interface FIFO. The TDC-F1 starts with channel no. 1. If headers are disabled, they won't be transferred to the output FIFO. Following time stamps are combined with the channel number and the chip address. Then they are written to the interface FIFO. Afterwards, if the output FIFO is empty or another header is following, the next channel is selected. As soon as all 8 channels are read out or the interface FIFO is full, the TDC-F1 starts to give out data into the external FIFO.

Relevant registers:	
Register:	0
Bits 0-15:	= '0' (disable headers and trailers)
Register:	15
Bit 1:	= '1' set common mode

2.5 Synchronous mode

The Synchronous mode is operating similar to a predivider for extension of the measurement range of the TDC-F1. For measurement tasks with time intervals longer than 7us the synchronous mode in combination with an external circuit can be used. In this mode there is no external start signal but a SYNCRES pulse (pin 52) that is synchronous to the reference clock. This is used to initialize an internal start, that indicates time zero. By means of this the TDC-F1 is generating it's own starts in constant intervals. The interval between starts can be programmed in multiples of the reference clock (register7 Refcnt) + 2. Setting also the common modebit in register 15, the internally created start signals can be observed at pin 1 'tokout'. This mode is typicially used together with trigger matching.

Relevant registers:	
Register:	7
Bits 6-14:	refstart-counter refcnt
Register:	15
Bit 2:	= '1' set synchronous mode

Example:

Setting the internal counter Refcnt = 38, the restart period is 1µs

2.6 Leading-Trailing ('Letra') Mode

Another mode specific to high energy physics is the leading-trailing mode. In this mode every channel is sensitive to rising and falling edges. The limitation for the pulse width is defined by the double pulse resolution of typ. 20ns (max. 30ns). The letra mode can be combined with any other measurement mode.

Additionally to the time stamp the kind of slope (rising or falling) is stored. The lowest one of the 16 data bits indicates the slope ('1' = rising edge. The resolution is bisected.

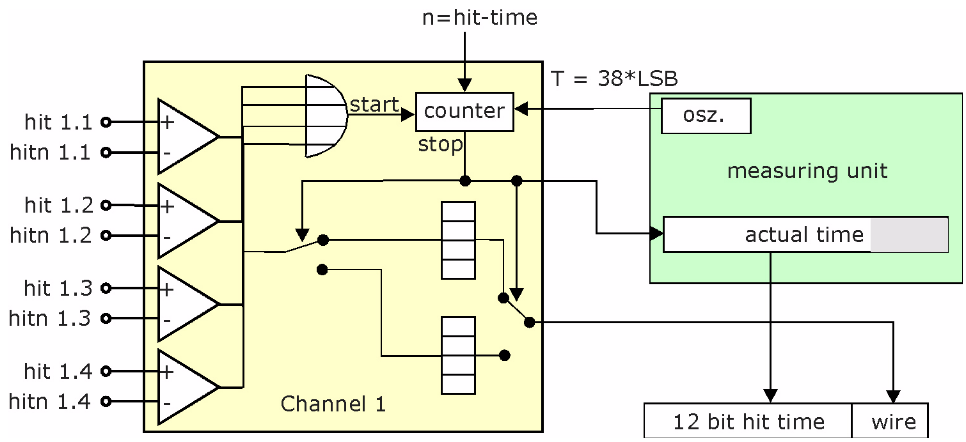
data word time measurement letramode	1	0	3 Bit Chip address	3 Bit Channel address	15 Bit Time	1 Bit Slope

Relevant registers:	
Register:	1
Bit 13:	'1' enables letra mode

2.7 Hit Mode

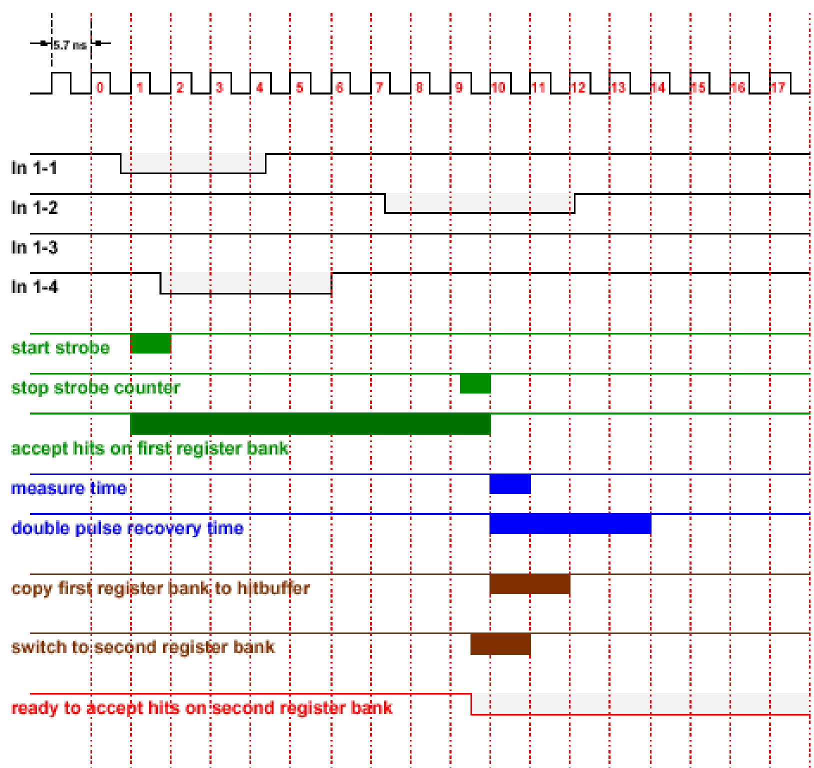
Another mode to operate the F 1-chip is the so called input register, latch or hit mode. This mode is selected by software during TDC initialization (register 1, bit 14). It is designed for the readout of detectors which do not require precise time information for event pattern reconstruction but only time stamps for event building in a pipelined data acquisition system or background suppression. Therefore it suits the requirements for MWPC readout or standard latch units and can be regarded as a cost efficient replacement of existing commercial products.

Figure 9 : Input structure hit mode



In the latch mode the number of input channels of the F 1 is increased to 32. Each group of four of the 32 channels is connected to two fourfold input buffers and a logic OR which is linked to one of the eight time measurement channels of the F 1. When a hit arrives on one of the four combined channels the next clock cycle of the asymmetric ring oscillator starts a 6 Bit counter. This counter, set in register 7 bits 0-5 ('hitt'), which defines the strobe length during which the registers accept input signals,

Figure 10 : Timing hit mode



is synchronous to the measuring unit and running with a period of 1LSB*38 ≈ 4.56ns, where LSB = 120ps refers to the digitization bin size of the F1 in the standard resolution mode. After a pre-set time of 4.56 ns < tstrobe < 292 ns (64*4.56 ns) (register 7, bits 0-5) the four inputs are switched to the second input buffer and a time stamp is taken with the full accuracy of the standard mode. The 12 most significant bits of the time stamp are placed in front of the four bits from the input register and transferred to the hit FIFO.

data word hit measurement	1	0	3 Bit Chip address	3 Bit Channel address	12 Bit Time	4 Bit wire address

To ensure that no hits are lost during the time when the input to the hit registers are switched both hit registers will accept signals during an overlap in time which is ≈ 2 ns. Although it is desirable to have the overlap as short as possible, small variations in production processes and the danger of efficiency gaps may require a longer overlap. The register overlap time can be doubled by software selection during initialization (register 1, bit 9 'ovlap').

Figure 8 shows an example in which three channels - channel one, two and four - had hits within the strobe window. In this example the pre-selected strobe time was set to 9*4.56ns = 41 ns. Measurements in the hit mode are only reasonable when the F 1 is switched to standard resolution and leading edge detection. The strobe length must be chosen longer than the double pulse resolution of the F 1 input stages. Otherwise measurements will end in efficiency gaps. The strobe counter is synchronous with a fixed clock cycle therefore the variation in the start of this counter introduces an uncertainty on the end of the strobe and the time measurement of 0< tstrobe < 4.56 ns.

2.8 High Resolution

For trigger mode and common mode it is possible to combine two neighbored channels (1+2, 3+4, 5+6, 7+8) to form a single channel with twice the resolution, typ. 60ps. As only 16 bit are available for the time stamp, the measurement range is bisected, typ. 3.9µs. Using high resolution mode, only 4 measuring channels are available. For the storage of the time stamps the hit FIFOs of both channels are used. The times stamps are stored alternately, starting after power-on reset on the odd numbered channel. In the data output stream first the time stamps of the odd numbered channel will be found, afterwards the hits of the even numbered channel.

Example:

Assume the F1 running in common mode, channel 1 active and four hits in intervals of 100ns given to stop input 1.

The data stream looks like:

ch1 100ns	*alternatively*	*ch1 200ns*
ch1 300ns		*ch1 400ns*
ch2 200ns		*ch2 100ns*
ch2 400ns		*ch2 300ns*

Combining two channels to one, the number of registers in the hit FIFO and the output FIFOs are doubled, also doubling the multihit capability.

If high resolution is selected, the even numbered channels associated to active channels must be enabled, too, connecting disable to GND and disablen to Vddio. Connect start to GND and startn to Vddio.

For a good performance, the two neighbored channels must be adjusted to each other. Therefore each channel can be delayed by a programmable value, set in registers 2-5. The structure of the measuring unit demands an adjustment of the start (channels 9 and 10), too (register 6).

The adjustment values may depend on the production process and can be requested from the members of acam. Currently the best results are achieved setting the adjustments to '0x3F' for channels 1,3,5,7,9 and to '0' for channels 2,4,6,8,10.

The high resolution mode can be realized externally, too, using normal resolution and setting the shift between the channels externally using resistors in series to the inputs. The delay between the channels must be > 1.5 LSB. The data must be averaged in a post processing. The advantage of this external construction is, that all eight channels can be combined to a single one. Also the data output is structured in a clear manner.

For hits on one of the channels the double pulse resolution is typ. 20ns (max. 30ns), for hits on different channels there is no limitation.

Relevant registers:	
Register:	1
Bit 15:	'1' sets high resolution mode
Registers:	2,3,4,5
Bits 0-5,8-13:	Adjust channels
Register:	6
Bits 0-5,6-11:	Adjust start channel

2.9 Data Output

The link to a receiver of TDC data is either realized via an 8 Bit/10Bit HOTLink protocol (CY7B923 and CY7B933 chips from Cypress [4]) with a maximum transmission rate of up to 50 MHz or directly via a 24 bit bus architecture, which can be clocked with a frequency of up to 50MHz.

HOTLINK

The HOTLink chip is a convenient device to serialize 8 bit data words. It has a capability of up to 50 MByte data transfer per second. For the data transfer by HOTLink the 24 bit hit information is split in three 8 bit words. The eight most significant bits are read out first, the least significant bit last. The timing of the data output is according to the specifications of the HOTLink and the clocked FIFO CY7C441/CY7C443 from Cypress Semiconductor.

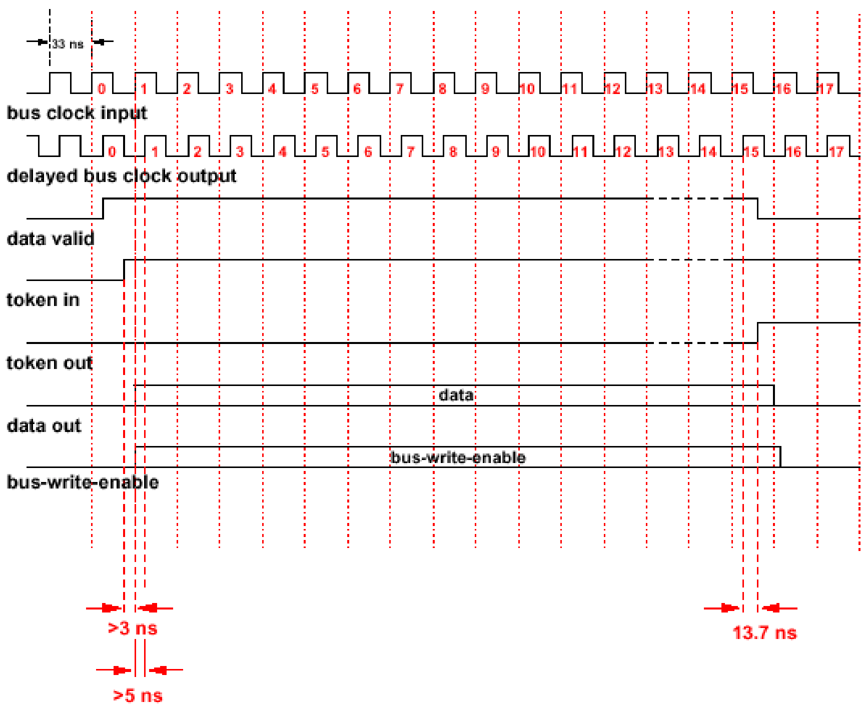


Figure 11: Timing token-controlled parallel bus

These circuits accept incoming data at their input with a positive edge of a bus clock, provided that the bus-write-enable signal was pulled down to zero at least 5 ns earlier. The data and the bus-write-enable signal, however, may change state immediately after the positive edge of the bus clock. After a token has been successfully received by a TDC, the data from the interface FIFO are applied to the TDC data-out pins synchronously to the bus clock (pin 157).

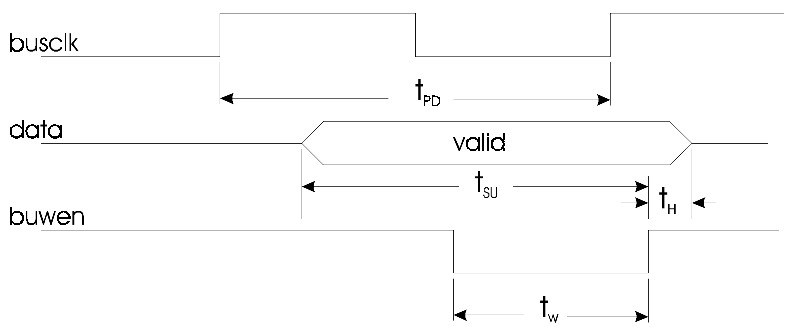
The TDC chip provides a special bus-write-enable (pin 6) and a delayed bus clock (pin 3) with a skew which is adjustable in the range of 3 to20 ns in 15 steps (register 6, bits 12-15) with respect to the input bus clock. For a safe timing the delayed bus clock from (pin 3) must be used to clock the HOTLink input. The bus-write-enable signal is applied only when valid data are at the output pins of the TDC. Up to eight F 1-chips can be connected to one HOTLink transmitter or FIFO. In this case all bus-write-enable pins must be connected together to the HOTLink or FIFO and a 2K7 pull-up resister must be applied. To ensure a flawless performance the time offset between all bus-clock inputs must be less than 1 ns.

Direct FIFO access

In common mode the easiest way to operate the TDC-F1 is to combine it with an external FIFO connected to the parallel data bus. The TDC-F1 writes the data directly into this FIFO. From there the data can be reprocessed by any kind of processor. The time interval between the arrival of the hits at the input and the output of data on the data bus is strongly dependent on the measurement rate. A single hit needs typically 800ns for internally processing. At maximum operating rate (app. 20 million measurements per second) the time interval may be 3300ns.

The following timing diagram shows how the TDC-F1 applies data to the data bus. To this the TDC-F1 sets the low-active WRITE strobe (pin 6, buwen). The timing is the same for 8 bit and 24 bit bus width.

Figure 12 : Timing parallel bus, direct access



Parameter	Symbol	min.	max.	Unit
Period bus clock (busclk)	t_{PD}	20		ns
Data setup time	t_{SU}	t_{PD}- 4		ns
Data hold time	t_H	1.4	7	ns
Pulse width of write strobes	t_W	0.5 * t_{PD}		ns

'buwen' shall be used as write strobe for the FIFO. Connect 'tok_in' to GND. Let 'tok_out' and 'busclko' be not connected.

Structure of output data when 24bit bus width is selected:

MSB	each MSB ... LSB			LSB
1	0	3 Bit Chip Address	3 Bit Channel Address	16 Bit Time Data
		MSB ... LSB	MSB ... LSB	MSB ... LSB

If 8bit bus width is selected, the mean significant byte will be sent first, the least significant byte at last.

Relevant registers:	
Register:	6
Bits 12-15:	busclkdelay
Register:	15
Bit 0:	select '0'=24bit / '1'=8 bit data output format

2.10 Serial Interface

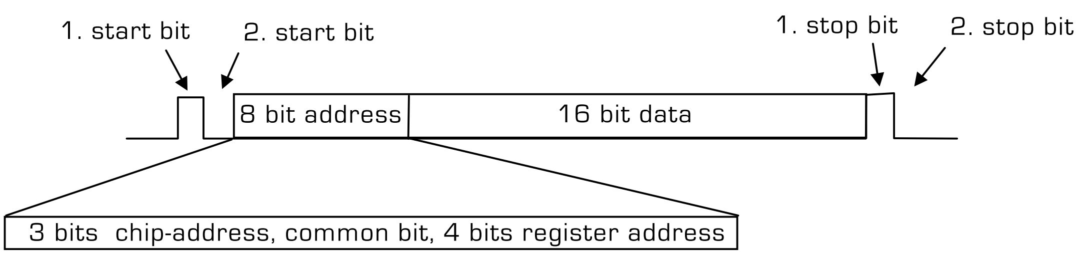
As the parallel interface is provided only for data output, the TDC-F1 has to be configured by means of the serial interface. The principal function is as follows:

In quiescent condition pin SIN must be set to '0'. In this condition the current consumption of the interface is minimized as the biggest part of the circuit is disabled. The serial interface is activated by the first rising slope on pin SIN. This slope starts the fourfold oversampling unit. Afterwards the data frame must be sent to SIN with the correct bit length (see Figure). The bits must last for four periods of the clock relevant for the serial interface. Two Selections can be done for the clock. The level on pin SICLKON selects between the reference clock and the clock available at pin SICLK.

SICLKON	clock relevant for serial interface:
0	reference clock (REFCLK-input)
1	SICLK (SICLK-input)

If, starting with the second stop bit (falling slope at SIN), the serial interface received a correct data frame, the data will be transferred to the addressed register. For a correct data frame it is necessary that all the start and stop bits are of the correct polarity, that all the bits could be detected correctly and that the common bit in the frame was '1'. The common bit '1' indicates the TDC-F1 to accept data regardless of the chip address. If the common bit is '0', the TDCF1 accepts data only, if the chip address code in the data frame corresponds to the chip address programmed at the pins (pins 44-46). This makes sense only in multi chip operation. Common bit register address and data must have the following format. (All serial data: MSB ... LSB)

Figure 13 Timing serial Interface



Successive data frames can be attached together without delay.

There is another possibility to address the serial interface when SICLKON is set to '1'. It is not necessary to give a continuous clock to this pin. The data can be transferred bit by bit. It is possible to configure the TDC-F1 with only two processor ports.

This is realized in the following manner:
The rising slope of the first start bit activates the serial interface. After this, send four positive pulses with any pulse width (only the rising slope is important). Afterwards give the next bit to pin SIN and send again four pulses to SICLK. Repeat this for the complete data frame.

2.11 DAC

The TDC-F1 offers a serial interface for direct control of the 8-fold D/A-converters AD8841 or AD8842 from Analog Devices. The DAC can be used to set the trigger levels for the differential stop inputs independently.

Eight byte of data can be written into registers 11 - 14. The data transfer to the DAC is initialized by setting bit 0 in register 1 (DA). After finishing the data transfer the TDC-F1 will clear the DA bit itself.

Relevant Registers:	
Registers:	11-14
Bits 0-15:	digital values for DAC AD8842
Register:	1
Bit 0:	DA, '1' starts data transfer to DAC, is reset automatically

3 Measuring Results

The following pages show the real performance of the TDC-F1. The power and the limits of the device are pointed out. All results presented here are evaluated with the prototypes of the TDC-F1 implemented in the ATMD measurement system.

3.1 The Terms 'Precision' and 'Resolution'

At first, we want to make some remarks on the meaning of the two terms.

When talking about resolution, we mean the smallest digital unit or LSB of the time-to-digital converter (in analogy to ADCs). This is in conformity with electronics' usage and different to scientific usage where it is called BIN.

The precision of a measuring is defined by different parameters, in detail:

3.1.1 Standard Deviation

The standard deviation is the standard square fault about a row of measurement results to the arithmetical mean average value of these measurement results. It is a good value for the noise which is caused by quantization effects and other randomly distributed sources of inaccuracy. If the assumption of statistically distributed results is fulfilled, the standard deviation can be decreased by averaging with the square root of the number of samples.

For example: If it is possible to take the average value of 100 measurements, the standard deviation of these value will be 1/10th (square root of 100) of the standard deviation of a single value.

3.1.2 Systematic Errors

Systematic errors belong to measured values that appear at the same point of the characteristic curve for the time. When measuring the same time interval, also the measuring errors have the same quantity.

Values with systematic errors aren't distributed around the averaged value by chance. Therefore these errors can't be eliminated by averaging. They are the 'more unpleasant' faults which are very heavy to remove.

3.1.3 Offset Errors

The offset error is a constant error value which is added/subtracted from the measuring value over the complete measuring range. Offset errors belong to the systematic errors, but nevertheless they are described separately.

3.2 Attainable Standard Deviations of the TDC-F1

The following standard deviations of the single measurement results can be expected:

- normal resolution with resolution adjust: ca. 0,7 - 0,8 LSBs
- high resolution with resolution adjust: ca. 0,8 - 0,9 LSBs

Please note:

These values can be drastically improved using averaging. (as mentioned above)

Optimal stochastic prerequisites are available with resolution adjust. In this mode it is possible by averaging to increase the precision of the result considerably. **A standard deviation of less than 1 ps can be achieved**. It isn't necessary that the incoming signal is noisy. The F1 produces the necessary statistics by itself in this mode.

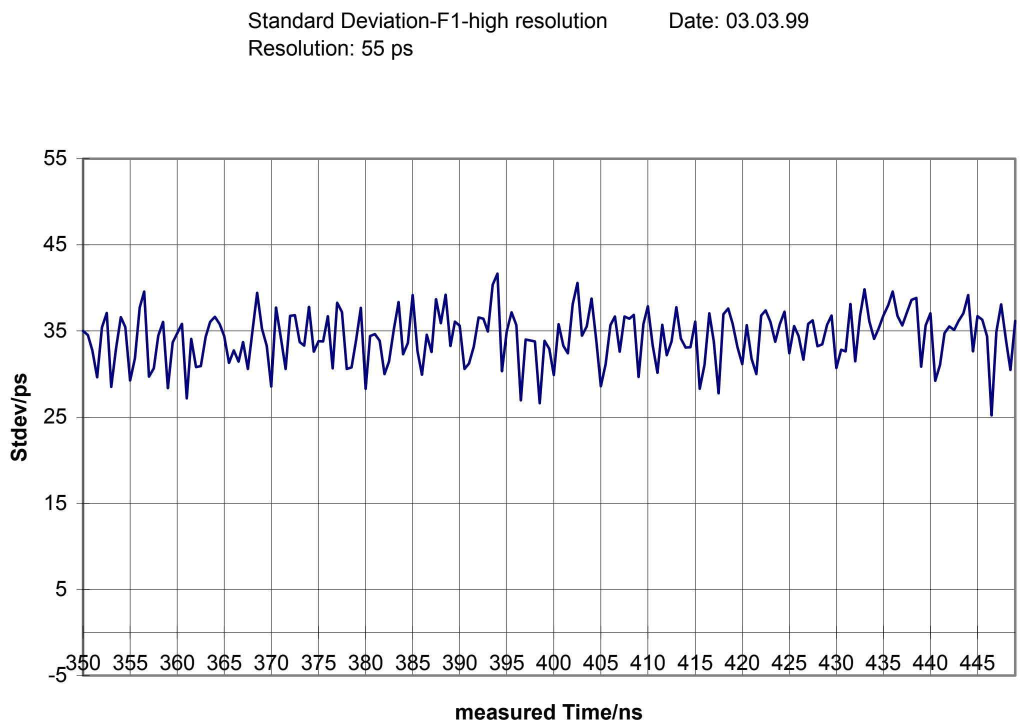
3.3 Offset Errors of the TDC-F1

It a hit is supplied simultaneously to all pins, the measurement value will not be the same for all channels. Because of the different on-chip wire lengths for the different channels, you get slightly varying offsets. The offsets also vary strongly with different input threshold voltages and slightly with the set resolution. With the same threshold voltage on all channels the maximum offset between the channels is 400ps. If you need offset-free measurements over all channels, you can put a resistor of 5-30 Ohm in front of the inputs to adjust each channels offset. The serial resistors together with the input capacities of the pins form a R-C-networks defining the delays.

The offsets however are very stable and vary less than 0.1 LSB with temperature over the whole temperature range.

3.4 Systematic Errors of the TDC-F1

Figure 14



Above diagram shows the measured deviation of the TDC-F1 in comparison to a reference device in the time domain of 115-350 ns. The TDC-F1 was driven with resolution adjust and high resolution. To be able to recognize systematical errors, high averaging rates are necessary to filter out the effects of quantization noise. An averaging rate of 10.000 was chosen. Note the subdivision of the Y-axis into 5ps/Div.

3.5 Histograms

For some applications in research the TDC-F1 is used for the building of histograms. In this case the differential non-linearity (DNL) is primarily of great importance.

Due to the nature of digital TDCs, the DNL is not so good, but strongly periodical by 2. Figure 15 shows a histogram with normal resolution and resolution adjust. Clearly the periodicity of the width of the single LSBs can be recognized. A narrow LSB follows a broad LSB and vice versa. The DNL can be dramatically improved omitting the LSB of the time stamps. The resolution will be only the half, but the DNL will be less than 1%.

The differential non-linearity is also dependent on the voltage difference between core and measuring unit, which is in correlation to the adjusted resolution (see Figure- Figure 17).

- Channel 1, Normal resolution, different adjustments for resolution

(number of hits versus channel number)

Figure 15 Normal Resolution: 150,38ps Ch1

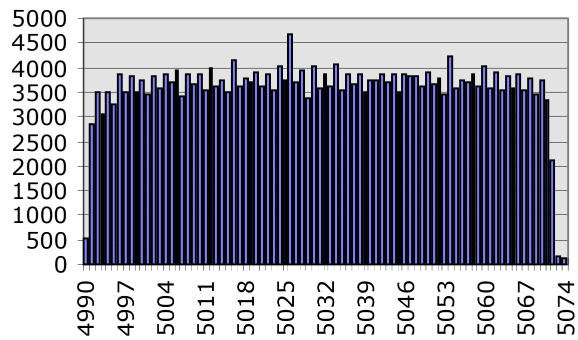


Figure 17 Normal Resolution: 113,19ps Ch1

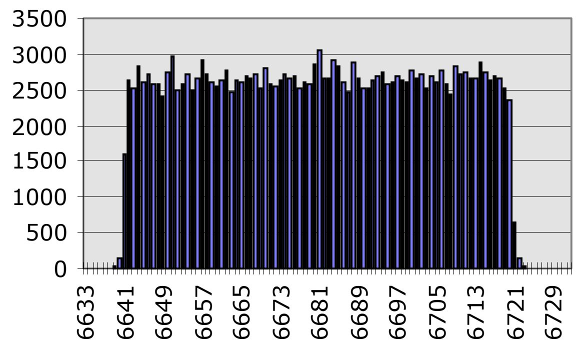
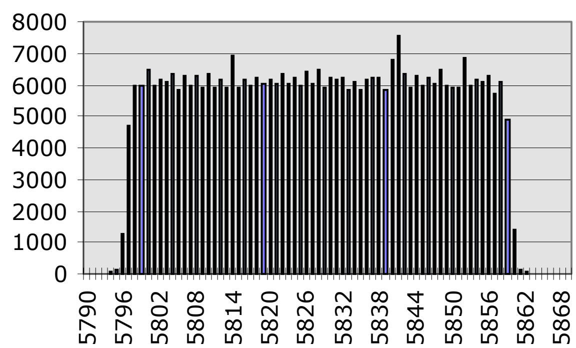


Figure 16 Normal Resolution: 131,58ps Ch1



- Channel 1, High resolution, different adjustments for resolution

Figure 18 High Resolution: 58,48ps Ch1

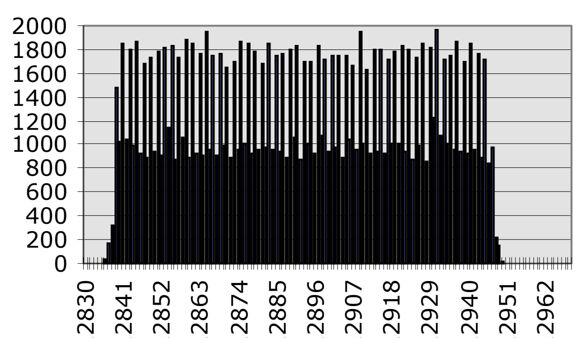
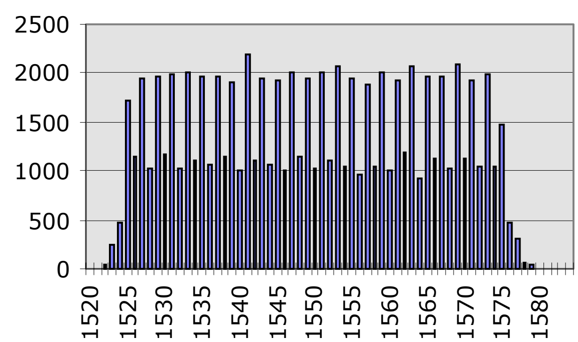


Figure 19 High Resolution: 65,79ps Ch1



- Different channels, High resolution, different adjustments for resolution

Figure 20 High Resolution: 65,79ps Ch5

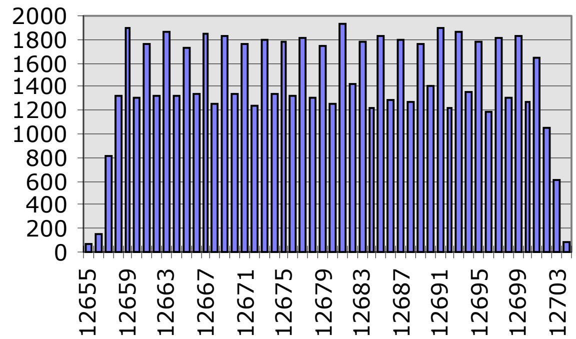


Figure 21 High Resolution: 65,79ps Ch3

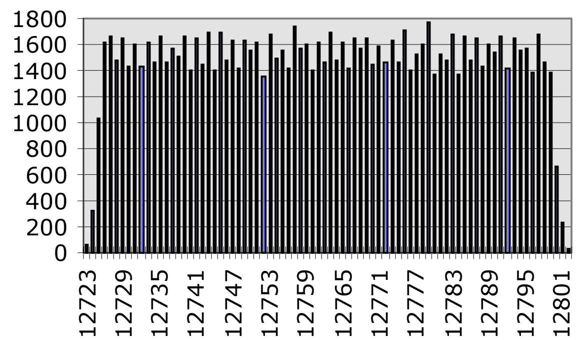
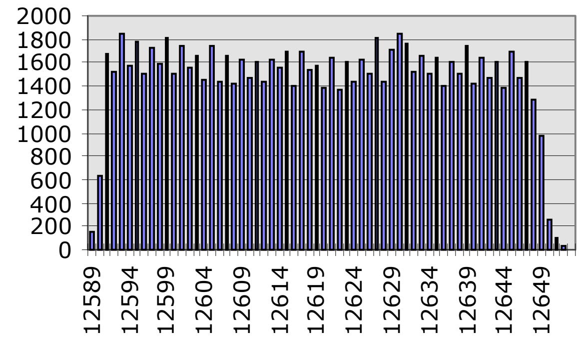


Figure 22 High Resolution: 65,79ps Ch7



4 Applications

will follow!

5 Technical Data

5.1 Electrical characteristics

There is no guarantee for correct functionality when operated above these ratings

Parameter	Symbol	min.	max.	Unit
Supply voltage Core	Vddc	2.7	5.5	V
Supply voltage measurement core	Vddh	2.7	5.5	V
Supply voltage pad ring	Vddio	2.7 >Vddc - 0.5V !	5.5	V
Supply voltage Outputs	Vddo	2.7 >Vddc - 0.5V !	5.5	V
HI Input voltage TTL-inputs	Vih	2.0	Vdd	V
LOW Input voltage TTL-Inputs	Vil	0	0.8	V
Input Rise/Fall Time	tr, tf	0	200	ns
Ambient Temperature	Ta	-40	+85	C

5.2 Absolute ratings

Operation above theses ratings may destroy the circuit

Parameter	Symbol	min.	max.	Unit
Supply voltage	Vddc/h Vddio Vddo	-0.3	7.0	V
Signal input voltages	Vi	-0.3	Vddio+0.3	V
Pin input current	Ii	-10.0	+10.0	mA
Storage temperature	Tst	-55	+125	°C
Solder temperature	Tl		300	°C for 10 sec.

5.3 Current consumption

The typical current consumption of the circuit will be (@ 5V 25 C)

Quiescent current: typ. 70 mA

Operating current: typ. 100mA. At extremely high measurement rates this may increase to 120mA.

5.4 Timings

The timings of the circuit, inclusive the resolution without resolution adjust mode, are influenced by three parameters.

- Process tolerances

- Supply voltage
- Temperature

The resulting timings are calculated as

$$Tpd = T_{pd}(typ.) * K_p * K_v * K_T$$

Kp = process influence
Kv = voltage dependency
KT = temperature dependency

The dependency on changes in production process is given in Table 2 Kp.

Process parameter	Value
Best-Case	0.61
Typical	1.0
Worst-Case	1.4

Table 2 Kp process dependency

Temp	Kt
125 C	1.26
85 C	1.15
70 C	1.11
25 C	1.00
-25 C	0.87
-40 C	0.82
-55 C	0.79

Table 3 Kt temperature dependency

VDD	Kv
5.5 V	0.94
5.0 V	1.00
4.5V	1.07
3.3 V	1.39
3.0 V	1.54
2.7 V	1.74

Table 4 Kv supply voltage dependency

Taking into consideration all these influences the resulting resolution of the TDC-F1 is:

Best-Case	(-40 C, 5.5 V, Best-Case Process):	72 ps
Typical	(25 C, 5 V , typical proxies):	120 ps
Worst-Case	(85 C, 4.5 V, Worst-Case Process):	168 ps

Take these tables to calculate the possible resolution under your operating conditions.

Example: The core supply voltage shall be 4V at 25 °C allowing to keep the resolution constant across the complete temperature range. Depending on the production lot the following resolution values should be taken into account:

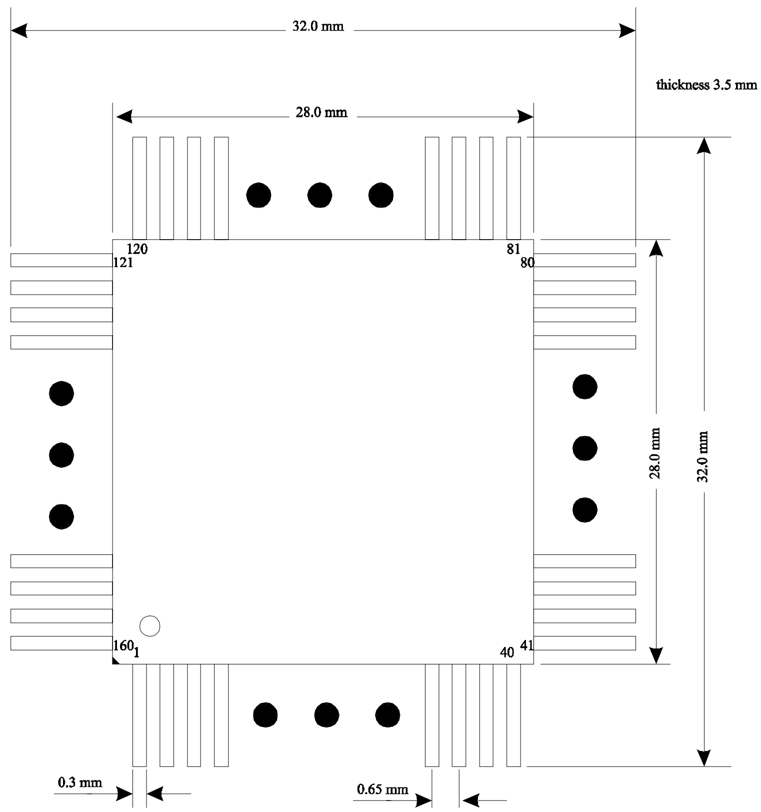
Best-Case:	Tpd= 150ps * 0.61* 1.20 * 1.0	= 110 ps
Typical:	Tpd= 150ps * 1.0 * 1.20 * 1.0	= 180 ps
Worst-Case:	Tpd= 150ps * 1.4 * 1.20 * 1.0	= 252 ps

Remark: The Kv Factor of 1.20 at 4 Volt was interpolated from Table 4 Kv.

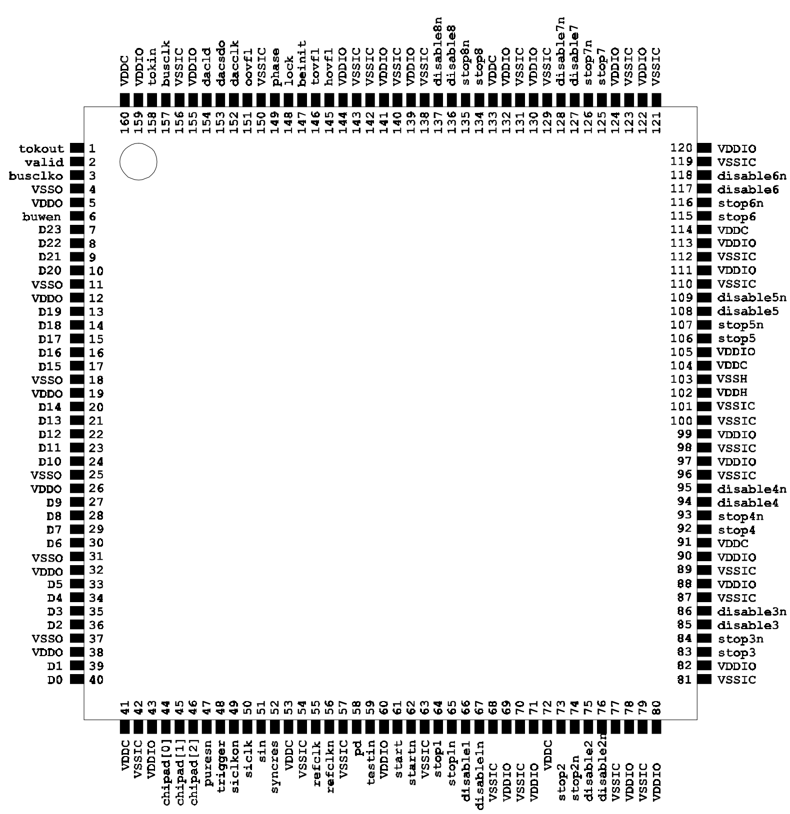
Such a big tolerance in production lots is the maximum guaranteed. Normally the tolerances are much less. For current production lots the tolerances in resolution varies between - 10% and + 10%. Within one production lot the tolerance is about ± 5% around the lot typical value.

5.5 Package

PQFP 160



5.6 Pinning



5.7 Pin description

Pin #	Name	Type	Description
1	tokout	Out - 8mA CMOS	Token out for multi chip operation
2	valid	out - 8mA CMOS	Indicates that data is available (high-active)
3	busclko	out - 12mA CMOS	Output delayed bus clock
4	VSSO	Supply	GND strong outputs
5	VDDO	Supply	Supply strong outputs
6	buwen	out - 16mA CMOS tristate	Bus-Write-Enable for data output(low-active)
7	D23	out - 16mA CMOS tristate	Data bit (most significant)
8	D22	out - 16mA CMOS tristate	Data bit
9	D21	out - 16mA CMOS tristate	Data bit
10	D20	out - 16mA CMOS tristate	Data bit
11	VSSO	Supply	GND strong outputs
12	VDDO	Supply	Supply strong outputs
13	D19	out - 16mA CMOS tristate	Data bit
14	D18	out - 16mA CMOS tristate	Data bit
15	D17	out - 16mA CMOS tristate	Data bit
16	D16	out - 16mA CMOS tristate	Data bit
17	D15	out - 16mA CMOS tristate	Data bit
18	VSSO	Supply	GND strong outputs
19	VDDO	Supply	Supply strong outputs
20	D14	out - 16mA CMOS tristate	Data bit
21	D13	out - 16mA CMOS tristate	Data bit
22	D12	out - 16mA CMOS tristate	Data bit
23	D11	out - 16mA CMOS tristate	Data bit
24	D10	out - 16mA CMOS tristate	Data bit
25	VSSO	Supply	GND strong outputs
26	VDDO	Supply	Supply strong outputs
27	D9	out - 16mA CMOS tristate	Data bit
28	D8	out - 16mA CMOS tristate	Data bit
29	D7	out - 16mA CMOS tristate	Data bit
30	D6	out - 16mA CMOS tristate	Data bit
31	VSSO	Supply	GND strong outputs
32	VDDO	Supply	Supply strong outputs
33	D5	out - 16mA CMOS tristate	Data bit
34	D4	out - 16mA CMOS tristate	Data bit
35	D3	out - 16mA CMOS tristate	Data bit
36	D2	out - 16mA CMOS tristate	Data bit
37	VSSO	Supply	GND strong outputs
38	VDDO	Supply	Supply strong outputs
39	D1	out - 16mA CMOS tristate	Data bit

40	D0	out - 16mA CMOS tristate	Data bit (least significant)
41	VDDC	Supply	Supply core
42	VSSIC	Supply	GND core and pad ring
43	VDDIO	Supply	Supply pad ring
44	chipad0	in - TTL	Chip address Bit0
45	chipad1	in - TTL	Chip address Bit1
46	chipad2	in - TTL	Chip address Bit2
47	puresn	in - TTL	Power-Up-Reset (low-active)
48	trigger	in - TTL	Trigger for measurement window (Filter function)
49	siclkon	in - TTL	Clock selection for serial interface (0 = reference clock , 1 = siclk)
50	siclk	in - TTL	Clock input for serial interface
51	sin	in - TTL	Input for serial data stream
52	syncres	in - TTL	Reset input for synchronous mode (GND if not used)
53	VDDC	Supply	Supply core
54	VSSIC	Supply	GND core and pad ring
55	refclk	in - differential positive	Reference clock input positive slope
56	refclkn	in - differential negative	Reference clock input negative slope
57	VSSIC	Supply	GND core and pad ring
58	pd	in - TTL	Power-Down for differential inputs (high-active)
59	testin	in - TTL	Selector for chip tester mode (high-active)
60	VDDIO	Supply	Supply pad ring
61	start	in - differential positive	Start input positive slope
62	startn	in - differential negative	Start input negative slope
63	VSSIC	Supply	GND core and pad ring
64	stop1	in - differential positive	Stop1 input positive slope
65	stop1n	in - differential negative	stop1 input negative slope
66	disable1	in - differential positive	Disable1 input positive slope
67	disable1n	in - differential negative	Disable1 input negative slope
68	hit1-3	in - differential positive	Hit input positive slope -> connect to VSSIC
69	hit1-3n	in - differential negative	Hit input negative slope -> connect to VDDIO
70	hit1-4	in - differential positive	Hit input positive slope -> connect to VSSIC
71	hit1-4n	in - differential negative	Hit input negative slope -> connect to VDDIO
72	VDDC	Supply	Supply core
73	stop2	in - differential positive	Stop2 input positive slope
74	stop2n	in - differential negative	Stop2 input negative slope
75	disable2	in - differential positive	Disable2 input positive slope
76	disable2n	in - differential negative	Disable2 input negative slope
77	hit2-3	in - differential positive	Hit input positive slope -> connect to VSSIC
78	hit2-3n	in - differential negative	Hit input negative slope -> connect to VDDIO
79	hit2-4	in - differential positive	Hit input positive slope -> connect to VSSIC

80	hit2-4n	in - differential negative	Hit input negative slope -> connect to VDDIO
81	VSSIC	Supply	GND core and pad ring
82	VDDIO	Supply	Supply pad ring
83	stop3	in - differential positive	Stop3 input positive slope
84	stop3n	in - differential negative	Stop3 input negative slope
85	disable3	in - differential positive	Disable3 input positive slope
86	disable3n	in - differential negative	Disable3 input negative slope
87	hit3-3	in - differential positive	Hit input positive slope -> connect to VSSIC
88	hit3-3n	in - differential negative	Hit input negative slope -> connect to VDDIO
89	hit3-4	in - differential positive	Hit input positive slope -> connect to VSSIC
90	hit3-4n	in - differential negative	Hit input negative slope -> connect to VDDIO
91	VDDC	Supply	Supply core
92	stop4	in - differential positive	Stop4 input positive slope
93	stop4n	in - differential negative	Stop4 input negative slope
94	disable4	in - differential positive	Disable4 input positive slope
95	disable4n	in - differential negative	Disable4 input negative slope
96	hit4-3	in - differential positive	Hit input positive slope -> connect to VSSIC
97	hit4-3n	in - differential negative	Hit input negative slope -> connect to VDDIO
98	hit4-4	in - differential positive	Hit input positive slope -> connect to VSSIC
99	hit4-4n	in - differential negative	Hit input negative slope -> connect to VDDIO
100	VSSIC	Supply	GND core and pad ring
101	VSSIC	Supply	GND core and pad ring
102	VDDH	Supply	Supply measurement core
103	VSSIC	Supply	GND measurement core
104	VDDC	Supply	Supply core
105	VDDIO	Supply	Supply pad ring
106	stop5	in - differential positive	Stop5 input positive slope
107	stop5n	in - differential negative	Stop5 input negative slope
108	disable5	in - differential positive	Disable5 input positive slope
109	disable5n	in - differential negative	Disable5 input negative slope
110	hit5-3	in - differential positive	Hit input positive slope -> connect to VSSIC
111	hit5-3n	in - differential negative	Hit input negative slope -> connect to VDDIO
112	hit5-4	in - differential positive	Hit input positive slope -> connect to VSSIC
113	hit5-4n	in - differential negative	Hit input negative slope -> connect to VDDIO
114	VDDC	Supply	Supply core
115	stop6	in - differential positive	Stop6 input positive slope
116	stop6n	in - differential negative	Stop6 input negative slope
117	disable6	in - differential positive	Disable6 input positive slope
118	disable6n	in - differential negative	Disable6 input negative slope
119	hit6-3	in - differential positive	Hit input positive slope -> connect to VSSIC
120	hit6-3n	in - differential negative	Hit input negative slope -> connect to VDDIO

121	hit6-4	in - differential positive	Hit input positive slope -> connect to VSSIC
122	hit6-4n	in - differential negative	Hit input negative slope -> connect to VDDIO
123	VSSIC	Supply	GND for core and pad ring
124	VDDIO	Supply	Supply pad ring
125	stop7	in - differential positive	Stop7 input positive slope
126	stop7n	in - differential negative	Stop7 input negative slope
127	disable7	in - differential positive	Disable7 input positive slope
128	disable7n	in - differential negative	Disable7 input negative slope
129	hit7-3	in - differential positive	Hit input positive slope -> connect to VSSIC
130	hit7-3n	in - differential negative	Hit input negative slope -> connect to VDDIO
131	hit7-4	in - differential positive	Hit input positive slope -> connect to VSSIC
132	hit7-4n	in - differential negative	Hit input negative slope -> connect to VDDIO
133	VDDC	Supply	Supply core
134	stop8	in - differential positive	Stop8 input positive slope
135	stop8n	in - differential negative	Stop8 input negative slope
136	disable8	in - differential positive	Disable8 input positive slope
137	disable8n	in - differential negative	Disable8 input negative slope
138	hit8-3	in - differential positive	Hit input positive slope -> connect to VSSIC
139	hit8-3n	in - differential negative	Hit input negative slope -> connect to VDDIO
140	hit8-4	in - differential positive	Hit input positive slope -> connect to VSSIC
141	hit8-4n	in - differential negative	Hit input negative slope -> connect to VDDIO
142	VSSIC	Supply	GND for core and pad ring
143	VSSIC	Supply	GND for core and pad ring
144	VDDIO	Supply	Supply pad ring
145	hovfl	out - 2mA CMOS	Hit FIFO overflow flag (high-active)
146	tovfl	out - 2mA CMOS	Trigger FIFO overflow flag (high-active)
147	beinit	out - 16mA CMOS tristate	Initialization flag (high-active)
148	lock	out - 2mA CMOS	Indicates lock of resolution adjust unit (high-active)
149	phase	out - 8mA CMOS	Phase output of PLL
150	VSSIC	Supply	GND for core and pad ring
151	oovfl	out - 2mA CMOS	Output FIFO overflow flag
152	dacclk	out - 2mA CMOS	Clock output to DAC
153	dacsdo	out - 2mA CMOS	Data output to DAC
154	dacld	out - 2mA CMOS	Load strobe DAC
155	VDDIO	Supply	Supply pad ring
156	VSSIC	Supply	GND for core and pad ring
157	busclk	in - TTL	Clock input for parallel interface
158	tokin	in - TTL	Token input (sensitive to rising slope)
159	VDDIO	Supply	Supply pad ring
160	VDDC	Supply	Supply core

The following buffers have been used for the I/Os:

Name	Direction	Buffer type
DO23 .. DO0, BEINIT	OUTPUT	16 mA CMOS Tri State, slew controlled
TOKOUT, VALID, PHASE	OUTPUT	8 mA CMOS
BUSCLKO	OUTPUT	12 mA CMOS
HOVFL, TOVFL, LOCK, OOVFL,	OUTPUT	2 mA CMOS
DACCLK, DACSDO, DACLD	OUTPUT	2 mA CMOS
BUWEN	OUTPUT	16 mA CMOS Tri State
CHIPAD2 .. CHIPAD0, PURESN	INPUT	TTL
TRIGGER, SICLKON, SICLK, SIN,	INPUT	TTL
SYNCRES, PD, TESTIN, BUSCLK,	INPUT	TTL
TOKIN	INPUT	TTL
REFCLK, START, ALLE STOPS	INPUT	DIFFERENTIAL LOW VOLTAGE
ALL HIT-INPUTS	INPUT	DIFFERENTIAL LOW VOLTAGE

Attention!!

There are no pull-up or pull-down resistors at the input buffers or I/O buffers. All the inputs need to be connected. The data bus may not be floating for a longer period of time. Otherwise these buffers may oscillate, the current consumption will increase and the functionality of the TDC-F1 is not guaranteed. The pins of the data bus must be provided with 50KOhm pull-up resistors. The pins beinit and buwen need a 1Kohm pull-up resistor.

6. Quick Reference

6.1 Electrical Characteristic

Recommended Operating conditions

Parameter	Symbol	min.	max.	Unit
Supply voltage core	Vddc	2.7	5.5	V
Supply voltage measuring unit	Vddh	2.7	5.5	V
Supply voltage pad ring	Vddio	2.7 >Vdd-0.5	5.5	V
Supply voltage outputs	Vddo	2.7 >Vdd-0.5	5.5	V
Diff. Input Common mode voltage	Vcm	0.8	2.8	V
Diff. Input Diff. Voltage	Vdiff	140m Vcm > 1.0		V
		50m Vcm > 1.8		V
TTL Input Voltage	Vi	0	Vddio	V
TTL Input Hi Voltage	VIH	2.0	Vddio	V
TTL Input Lo Voltage	VIL	0	0.8	V
TTL Input Hysteresis	Vh			V
Input Rise/Fall Time	tr, tf	0	200	ns
Quiescent current	Iq	typ. 70		mA
Operating current	Is	typ. 100mA		mA
Output current				mA
Data,Buwen,Beinit			16	
Busclko			12	
Tokout,valid,phase			8	
rest			2	
Amb. Temperature	Ta	-40	+85	C

Absolute Maximum Ratings

Parameter	Symbol	min.	max.	Unit
Supply voltage	Vddc/h Vddio Vddo	-0.3	7.0	V
Input signal voltage	Vi	-0.3	VDD+0.3V	V
Input pin current		-10.0	+10.0	mA
Storage temperature	Tst	-55	+125	C
Lead temperature			300 (10s)	C

6.2 Pin Description

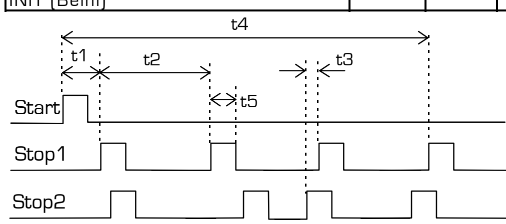
Pin	Symbol	Description
1	tokout	Token out
2	valid	data available
3	busclko	delayed busclock output
4,11,18, 25,31,37	Vsso	GND strong outputs
5,12,19, 26,32,38	Vddo	Supply strong outputs
6	buwen	Bus write enable
7-10,13-17,20-24, 27-30,33-36,39-40	D23-D0	Data
41,53,72,91,104, 114,133,160	Vddc	Supply core
42,54,57,63,81, 100,101,103,123, 142,143,150,156	Vssic	GND core and pad ring
43,60,82,105,124, 144,155,159	Vddio	Supply pad ring
44-46	chipadX	Chip address
47	puresn	Power-up-reset
48	trigger	Trigger input
49	siclkon	Clock select. ser.interface
50	siclk	Clock input ser, interface
51	sin	Input serial data
52	synres	Synchronous reset inp.
55,56	refclk	Reference clock inp.
58	pd	power down diff. inputs
59	testin	Test pin
61,62	start	Startinput
64,65	stop1	Stop 1 input
66,67	disable1	Disable 1 input
68,69	hit1-3	Hit 1-3 input
70,71	hit1-4	Hit 1-4 input
73,74	stop2	Stop 2 input
75,76	disable1	Disable 2 input
77,78	hit2-3	Hit 2-3 input
79,80	hit2-4	Hit 2-4 input
83,84	stop3	Stop 3 input
85,86	disable3	Disable 3 input
87,88	hit3-3	Hit 3-3 input
89,90	hit3-4	Hit 3-4 input
92,93	stop4	Stop 4 input
94,95	disable4	Disable 4 input
96,97	hit4-3	Hit 4-3 input
98,99	hit4-4	Hit 4-4 input
160,107	stop5	Stop 5 input
108,109	disable5	Disable 5 input
110,111	hit5-3	Hit 5-3 input
112,113	hit5-4	Hit 5-4 input
115,116	stop6	Stop 6 input
117,118	disable6	Disable 6 input
119,120	hit6-3	Hit 6-3 input
121,122	hit6-4	Hit 6-4 input
125,126	stop7	Stop 7 input
127,128	disable7	Disable 7 input
129,130	hit7-3	Hit 7-3 input
131,132	hit7-4	Hit 7-4 input
134,135	stop8	Stop 8 input
136,137	disable8	Disable 8 input
138,139	hit8-3	Hit 8-3 input
140,141	hit8-4	Hit 8-4 input
145	hovfl	Hit FIFO overflow
146	tovfl	Trigger FIFO overflow
147	beinit	Initialization flag
148	lock	PLL lock flag
149	phase	Phase output PLL
151	oovl	Output FIFO overflow
152,154	dacclk,-sdo,-ld	DAC Interface
157	busclk	Clock input paral. interface
158	tokin	Token input

6.3 Timings

Timings (@ 25°C, 5V):	min.	typ.	Max.	Unit
Resolution (LSB)		120		ps
Standard deviation				
Resolution adjust, normal res.		0.8		LSB
Resolution adjust, high resolution		0.9		LSB
Offset between channels			400	ps
Offset temperature drift			0.1	LSB

	min.	typ.	Max.	Unit
Integral non-linearity		0		LSB
Differential non-linearity				LSB
Resolution adjust, normal res.		10		%
Resolution adjust, high res.		50		%

	min.	typ.	Max.	Unit
Power-Up-reset	100			ns
INIT (Beini)				ns



Common mode, normal resolution:

	Timings (@ 25°C, 5V):	min.	typ.	Max.
t1	Minimum time difference		3.5ns	5ns
t2	Double pulse resolution one channel		20ns	30ns
t3	Double pulse resolution between 2 channels		0ns	
t4	Maximum time interval		65535*LSB	
t5	Minimum pulse width		2.5ns	4ns
	Number of channels		8	
	Number of hits per channel	4		

Common mode, high resolution:

	Timings (@ 25°C, 5V):	min.	typ.	Max.
t1	Minimum time difference		3.5ns	5ns
t2	Double pulse resolution one channel		20ns	30ns
t3	Double pulse resolution between 2 channels		0ns	
t4	Maximum time interval		65535*LSB	
t5	Minimum pulse width		2.5ns	4ns
	Number of channels		4	
	Number of hits per channel	8		

Trigger matching mode:

Timings (@ 25°C, 5V):	
trigger latency	> 300ns
Tframe = Tref * refcnt	< 0.9*Tframe
trigger window width	< 0.4*Tframe
trigger matching	typ.200ns +
nmax=largest number of hits	nmax*35ns

6.4 Registers

Register overview

<table>
<tr><th>Addr</th><th>D15</th><th>D14</th><th>D13</th><th>D12</th><th>D11</th><th>D10</th><th>D9</th><th>D8</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>0</td><td colspan="8">headen</td><td colspan="8">trailen</td></tr>
<tr><td>1</td><td>hires</td><td>hitm</td><td>letra</td><td colspan="2">sq</td><td>fake</td><td>ovlap</td><td colspan="2">ibs</td><td>obsp</td><td>m_in</td><td colspan="4">slow</td><td>DA</td></tr>
<tr><td>2</td><td>fe2</td><td>re2</td><td colspan="6">adjch2</td><td>fe1</td><td>re1</td><td colspan="6">adjch1</td></tr>
<tr><td>3</td><td>fe4</td><td>re4</td><td colspan="6">adjch4</td><td>fe3</td><td>re3</td><td colspan="6">adjch3</td></tr>
<tr><td>4</td><td>fe6</td><td>re6</td><td colspan="6">adjch6</td><td>fe5</td><td>re5</td><td colspan="6">adjch5</td></tr>
<tr><td>5</td><td>fe8</td><td>re8</td><td colspan="6">adjch8</td><td>fe7</td><td>re7</td><td colspan="6">adjch7</td></tr>
<tr><td>6</td><td colspan="4">busclkdel</td><td colspan="6">adjch10</td><td colspan="6">adjch9</td></tr>
<tr><td>7</td><td>beini</td><td colspan="9">refcnt</td><td colspan="6">hitt</td></tr>
<tr><td>8</td><td colspan="16">trigwin</td></tr>
<tr><td>9</td><td colspan="16">triglat</td></tr>
<tr><td>10</td><td>don1</td><td>pll</td><td>track</td><td>neg</td><td>r_adj</td><td colspan="3">refclkdiv</td><td colspan="8">hsdiv</td></tr>
<tr><td>11</td><td colspan="8">dac 2</td><td colspan="8">dac 1</td></tr>
<tr><td>12</td><td colspan="8">dac 4</td><td colspan="8">dac 3</td></tr>
<tr><td>13</td><td colspan="8">dac 6</td><td colspan="8">dac 5</td></tr>
<tr><td>14</td><td colspan="8">dac 8</td><td colspan="8">dac 7</td></tr>
<tr><td>15</td><td>don2</td><td>htest</td><td>stest</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>dia3</td><td>dia2</td><td>dia1</td><td>dia0</td><td>rosta</td><td>sync</td><td>com</td><td>8/24</td></tr>
</table>

Adr	Name	Description
0	headen	Enable header output
	trailen	Enable trailer output
1	hires	set high resolution mode
	hitm	set hit mode
	lerta	set Leading/trailing mode
	sq	safety bits, set to '0'
	fake	periodicity of fake triggers
	ovlap	overlap hit mode
	ibs	safety bits, set to '0'
	obspd	safety bits, set to '0'
	m_in	disable all signal inputs
	slow	safety bits, set to '0'
	DA	Start data transfer to DAC
2	fe2,1	activate falling edges chan.2,1
	re2,1	activate rising edges chan.2,1
	adjch2,1	delay adjustments chan. 2,1
3	fe4,3	activate falling edges chan.4,3
	re4,3	activate rising edges chan.4,3
	adjch4,3	delay adjustments chan. 4,3
4	fe6,5	activate falling edges chan.6,5
	re6,5	activate rising edges chan.6,5
	adjch6,5	delay adjustments chan. 6,5
5	fe8,7	activate falling edges chan.8,7
	re8,7	activate rising edges chan 8,7
	adjch8,7	delay adjustments chan. 8,7
6	busclkdel	delay for skewed bus clock
	adjch10,11	delay adjustments ref. chan.

Adr	Name	Description
7	beini	initialize chip
	refcnt	Set counter synchron. Mode
	hitt	strobe time for hit mode
8	trigwin	trigger window width
9	triglat	trigger latency
10	don1	diagnosis mode
	pll	test PLL
	track	cut regulation loop of PLL
	neg	invert phase output of PLL
	r_adj	switch on resolution adjust
	refclkdiv	reference clock divider PLL
	hsdiv	high speed divider PLL
11	dac 2,1	DAC data
12	dac 4,3	DAC data
13	dac 6,5	DAC data
14	dac 8,7	DAC data
15	don	diagnosis mode
	htest	for diagnosis purposes, set '0'
	stest	for diagnosis purposes, set '0'
	dia3	for diagnosis purposes, set '0'
	dia2	for diagnosis purposes, set '0'
	dia1	for diagnosis purposes, set '0'
	dia0	for diagnosis purposes, set '0'
	rosta	start ring oszillator
	sync	synchronous mode
	com	common mode
	8/24	8bit/24bit data output